Retrospective

Trace Cache: a Low Latency Approach to High Bandwidth Instruction Fetching
Eric Rotenberg, Steve Bennett, and James E. Smith

MICRO-29, Dec. 1996

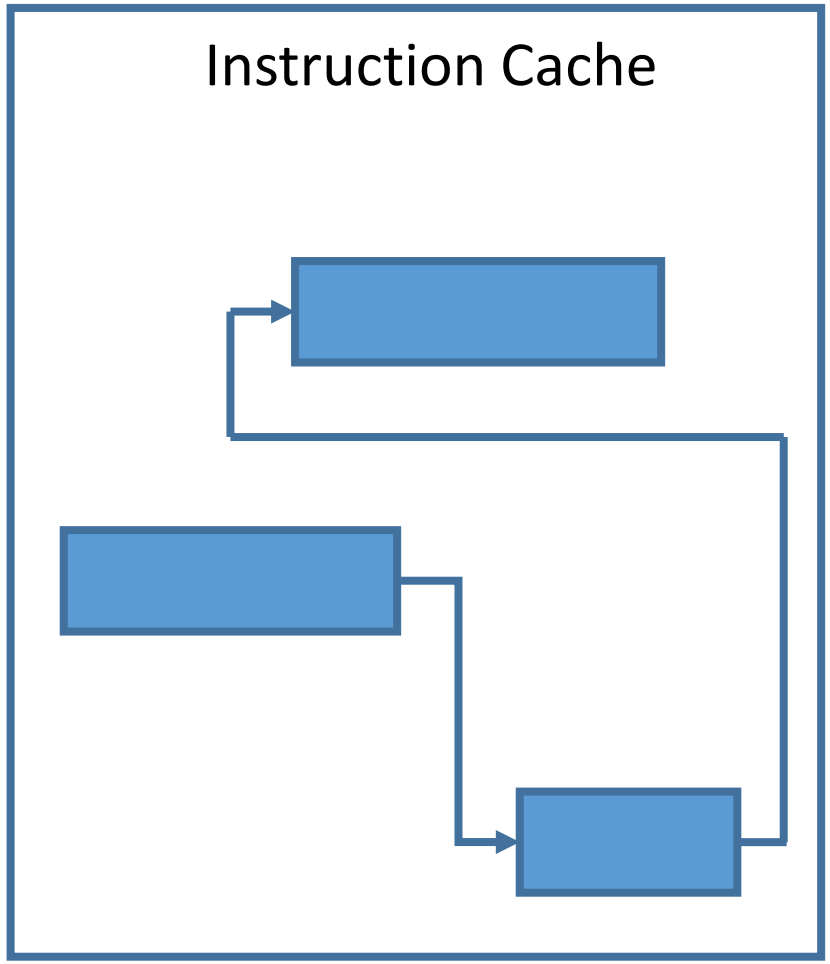
Concurrent Trace Cache Work

- Alexander Peleg and Uri Weiser. Dynamic Flow Instruction Cache Memory Organized Around Trace Segments Independent of Virtual Address Line. U.S. Patent 5,381,533, Filed Mar. 30, 1994, Issued Jan. 10, 1995.
- John D. Johnson. Expansion Caches for Superscalar Processors. Technical Report No. CSL-TR-94-630, Computer Systems Laboratory, Stanford University, June 1994.
- Sanjay Patel, Daniel Friendly, and Yale Patt. Critical Issues Regarding the Trace Cache Fetch Mechanism. University of Michigan, Technical Report CSE-TR-335-97, May 1997.
- Daniel Friendly, Sanjay Patel, and Yale Patt. Alternative Fetch and Issue Policies for the Trace Cache Fetch Mechanism. MICRO-30, Dec. 1997.

Genesis at UW-Madison

- Participated in Guri Sohi's group meeting (Todd Austin, Scott Breach, Andreas Moshovos, Avinash Sodani, T.N. Vijaykumar, …)
- Todd: SimpleScalar simulator's IPC limited by taken branches
- Jim: What if you could have a buffer that unrolls loops?
- Steve (post-meeting): familiar with the Branch Address Cache paper

Taken Branch Problem



Inspiration: Branch Address Cache

- Tse-Yu Yeh, Deborah T. Marr, and Yale N. Patt. Increasing the Instruction Fetch Rate via Multiple Branch Prediction and a Branch Address Cache. *7th Int'l Conf. on Supercomputing*, July 1993.

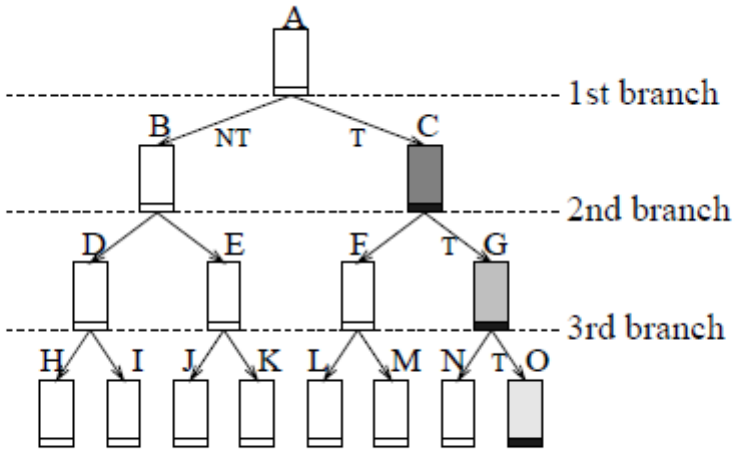


Figure 6. BAC stores subgraphs of the CFG.

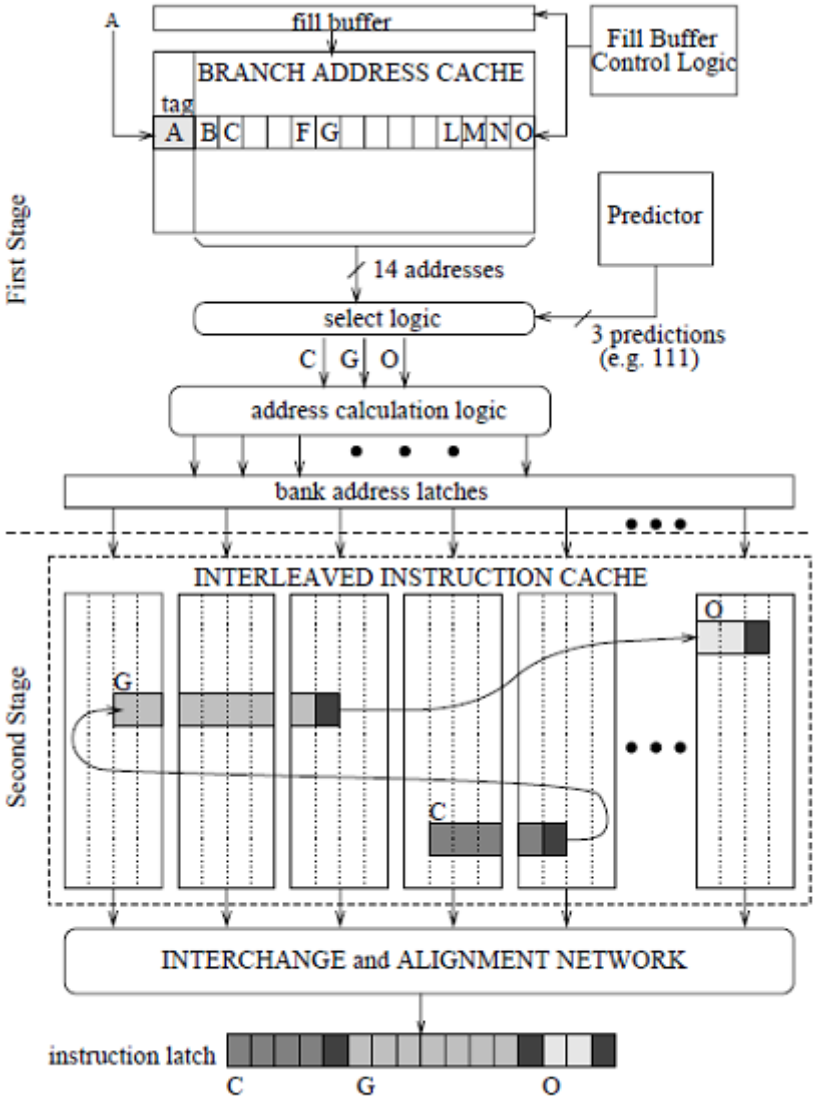
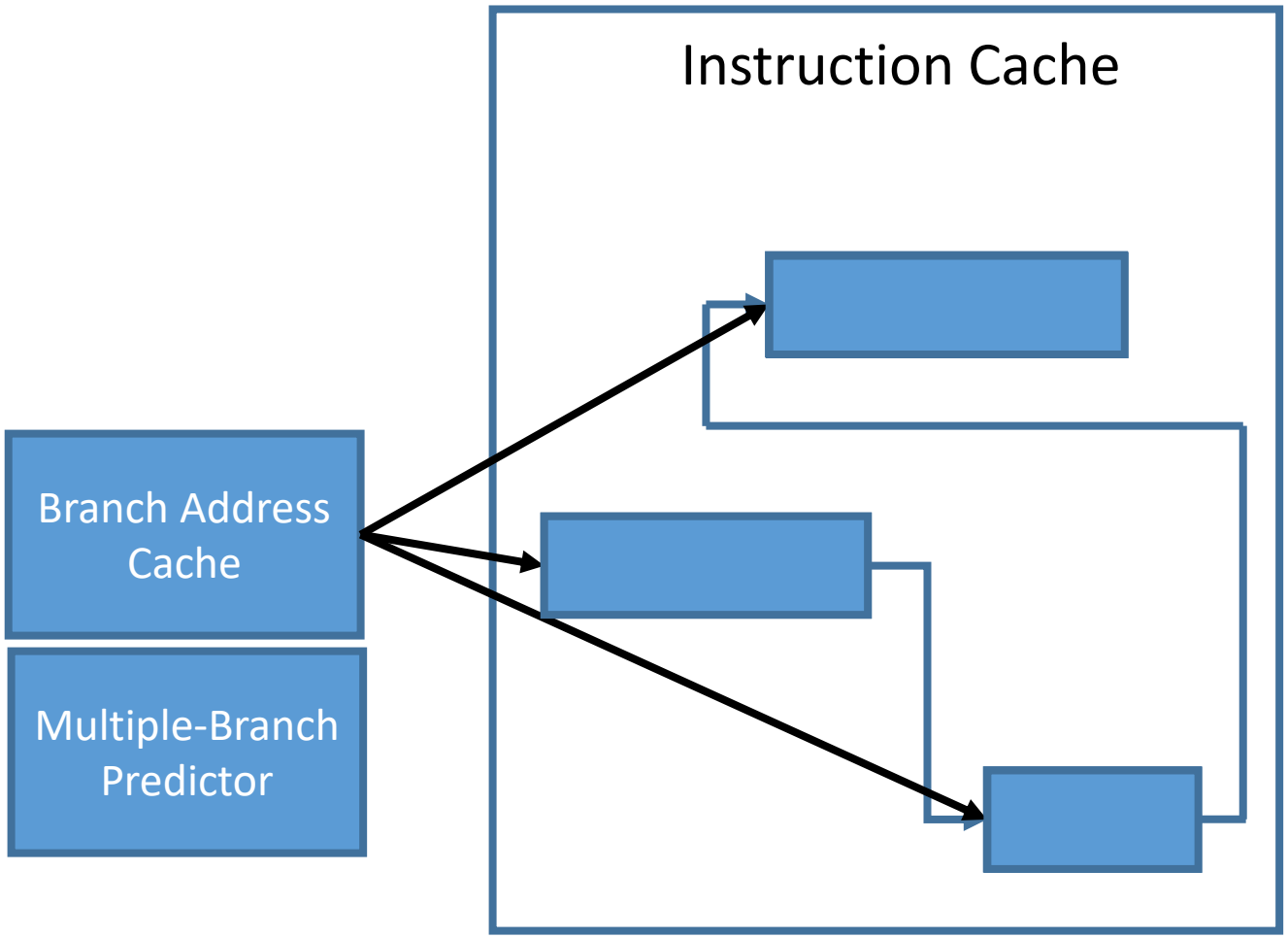
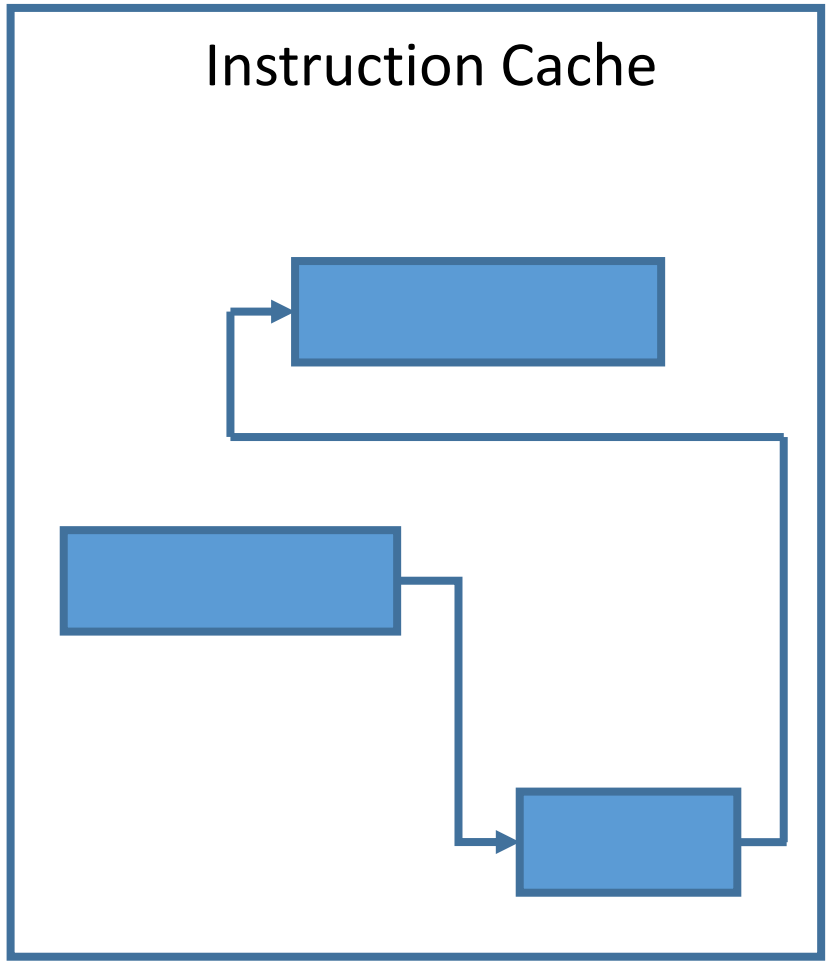


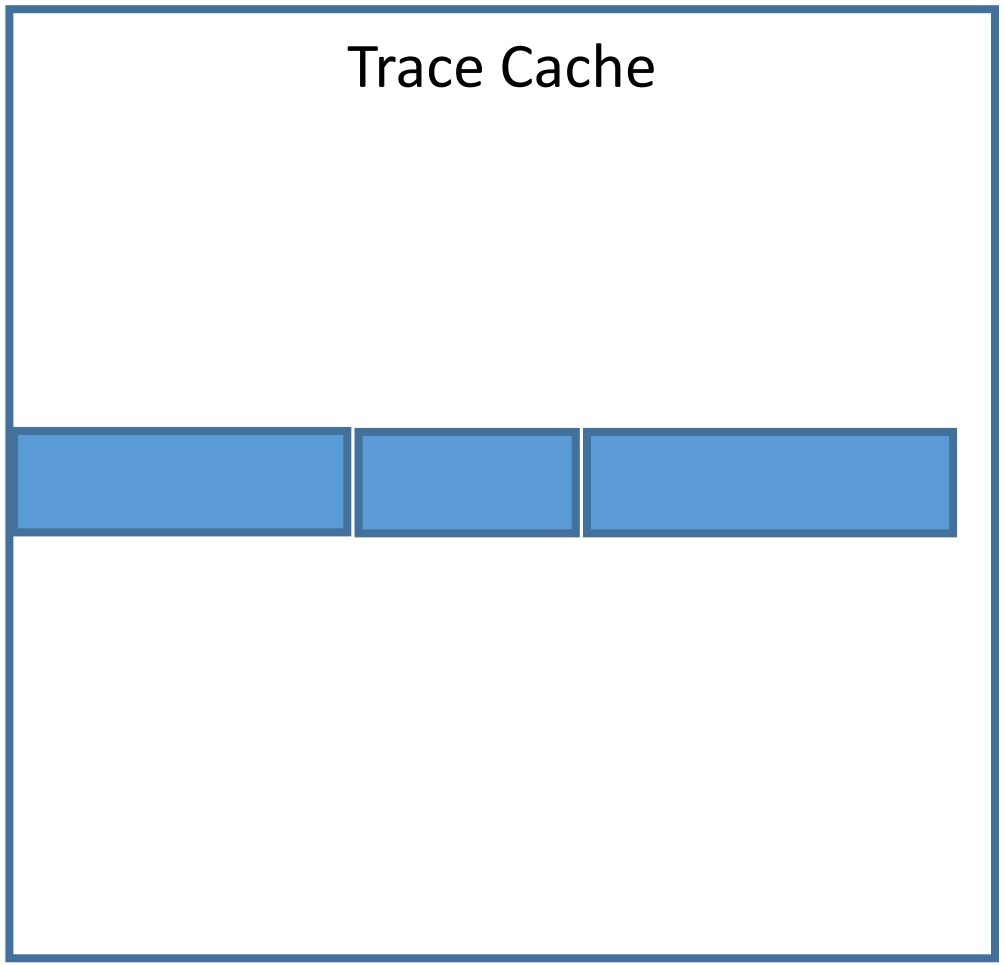
Figure 5. Branch address cache approach.

Assembling Traces On-the-fly



Trace Cache

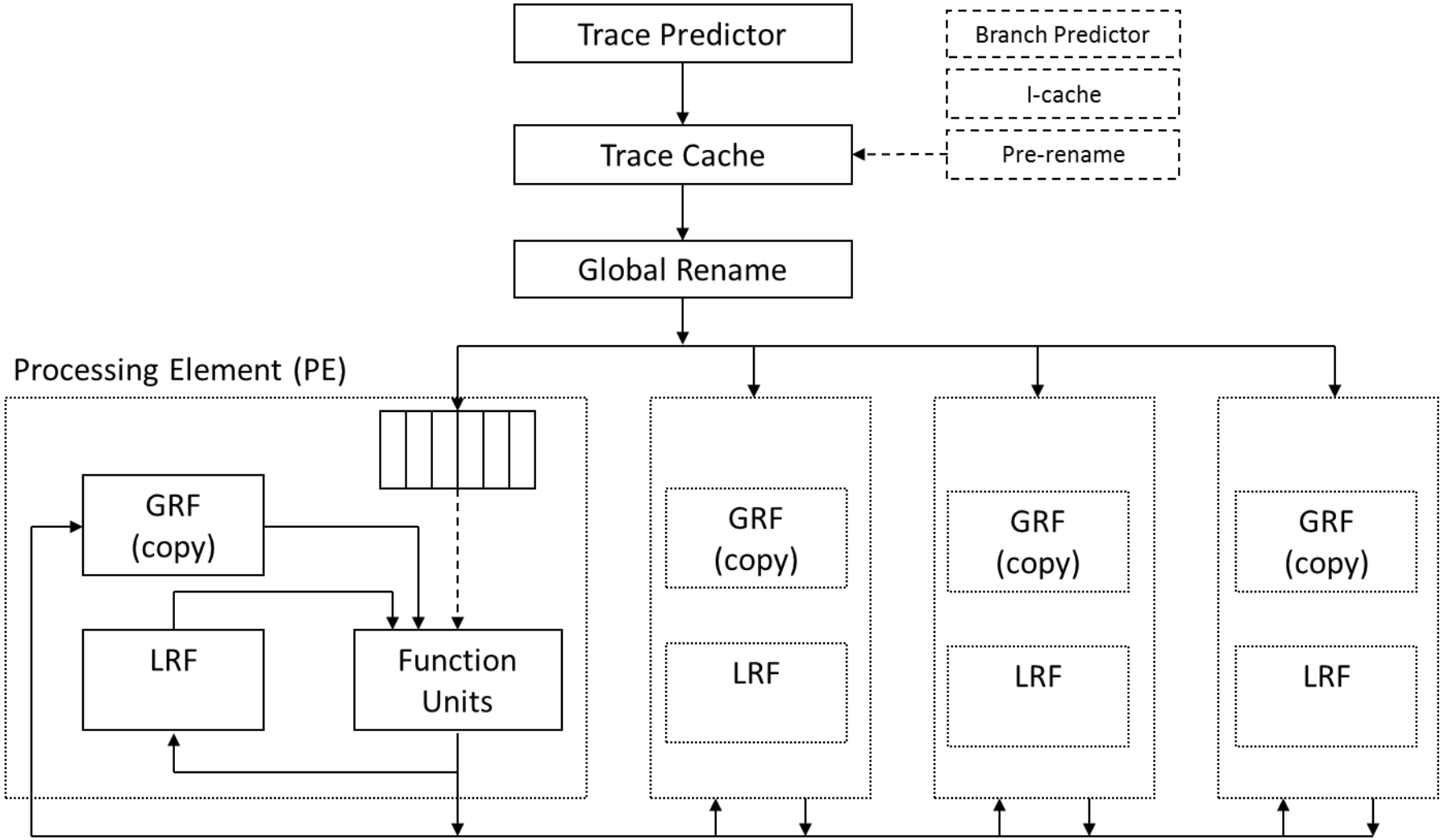




Interest in Trace Cache

- Rich design space
- New challenges
  - E.g., efficiency
  - E.g., multiple-branch prediction
- Processor paradigms shaped by trace cache
  - E.g., rePLay
    - S. J. Patel and S. S. Lumetta. rePLay: A Hardware Framework for Dynamic Optimization. IEEE Transactions on Computers, 50(6), June 2001.
  - E.g., Trace Processors
    - S. Vajapeyam and T. Mitra. Improving Superscalar Instruction Dispatch and Issue by Exploiting Dynamic Code Sequences. ISCA-24, June 1997.
    - J. E. Smith and S. Vajapeyam. Trace Processors: Moving to Fourth-Generation Microarchitectures. IEEE Computer, Sep. 1997.
    - E. Rotenberg, Q. Jacobson, Y. Sazeides, and J. E. Smith. Trace Processors. MICRO-30, Dec. 1997.

Trace Processor



The Future

- Recent neglect of wide superscalar processing is a research opportunity
- Revisit trace processors in context of past 15 years of innovation in control flow, data flow, store/load handling, and memory latency tolerance
- Revisit trace processors in context of Dark Silicon and Heterogeneous Multi-Core: risk is encouraged due to diverse microarchitectures on a chip