Call for Papers

The 52nd Annual IEEE/ACM International Symposium on Microarchitecture® (MICRO)

The International Symposium on Microarchitecture® (MICRO) is the premier forum for the presentation and discussion of new ideas in microarchitecture, compilers, hardware/software interfaces, and design of advanced computing and communication systems. The goal of MICRO is to bring together researchers in the fields of microarchitecture, compilers, and systems for technical exchange. The MICRO community has enjoyed having close interaction between academic researchers and industrial designers—we aim to continue and strengthen this longstanding tradition at the 52nd MICRO in Columbus, Ohio.

Important Dates

Abstract	March 29th, 2019 at 4:59 pm PDT
Full Paper	April 5th, 2019 at 4:59 pm PDT
First Round Decisions	June 1st, 2019
Rebuttal and Response	June 26th – July 3rd 2019
Notification	July 25th, 2019

We invite original paper submissions related to (but not limited to) the following topics:

- Architectures for emerging application domains such as deep learning, machine learning, relational computation, neuromorphic, quantum, etc.
- Accelerator designs and heterogeneous architectures including system-on-chip architectures, application specific fixed function, programmable, reconfigurable, near-data and in-memory accelerators, etc.
- Architectural support for security, side-channel attacks and mitigation, privacy preserving computation, IoT/Cloud/Cyber-Physical-System security, security primitives, trusted execution environments, etc.
- Architecture, microarchitecture and/or compiler optimizations for graphics processor units (GPUs) or other programmable accelerators.
- Microarchitecture and compiler techniques for optimizing the memory hierarchy, analysis of new memory hierarchies, emerging architectures based on new memory technologies.
- Hardware, software, and hybrid techniques for improving system performance, energy-efficiency, security, cost, complexity, programmer productivity, predictability, quality of service, reliability, dependability, scalability, etc.
- Architectures for instruction-level, thread-level, and memory-level parallelism: superscalar, VLIW, data-parallel, multithreaded, multicore, many-core, etc.
- Processor, memory, interconnect, and storage architectures.
- Compiler and microarchitectural techniques for parallelism (ILP, TLP, MLP).
- Microarchitecture techniques to better support system software, programming languages, programmability, and compilation.
- Advanced software/hardware speculation and prediction schemes.
- Microarchitecture modeling and simulation methodology.
- Low-power, high-performance, and cost/complexity-efficient architectures.

- Architectures for emerging embedded platforms, including smartphones, automotive, server/cloud, etc.
- Architecture and/or compiler optimizations for embedded processors, DSPs, ASIPs (network processors, multimedia, wireless, etc.).
- Insightful experimental and comparative evaluation and analysis of existing microarchitectures, hardware/software mechanisms and workloads.

Submissions should follow the guidelines and formatting rules specified on the conference website. Papers that violate these guidelines and rules may be returned to author(s) without review.