MichiganEngineering

ARM

RAS-Directed Instruction Prefetching (RDIP)

Aasheesh Kolli* **Ali Saidi†** **Thomas F. Wenisch***

* University of Michigan † ARM

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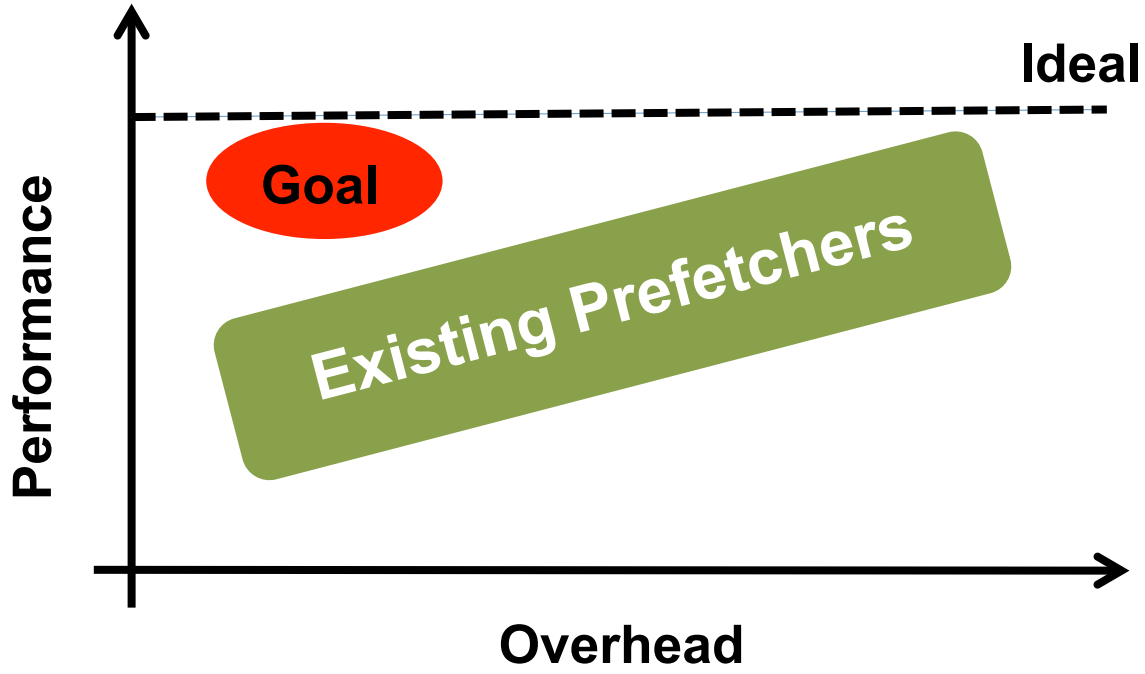
Why another instruction prefetcher?

- Poor I$ behavior affects modern workloads
- Cache size constraints → Prefetching



Our Goal: Low overhead, high accuracy instruction prefetcher

Contributions

- I$ misses correlate to program context
- Program contexts are repetitive → predictable
- RAS succinctly captures program context

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Performance improvement of 11.5%
Overhead of 64kB (3X ↓)