Virtually Aged Sampling DMR

Unifying Circuit Failure Prediction and Circuit Failure Detection

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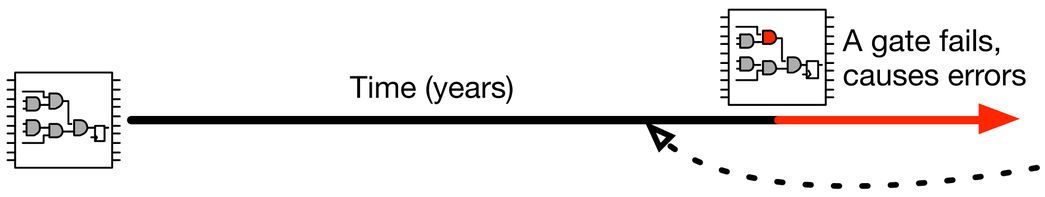
VERTICAL

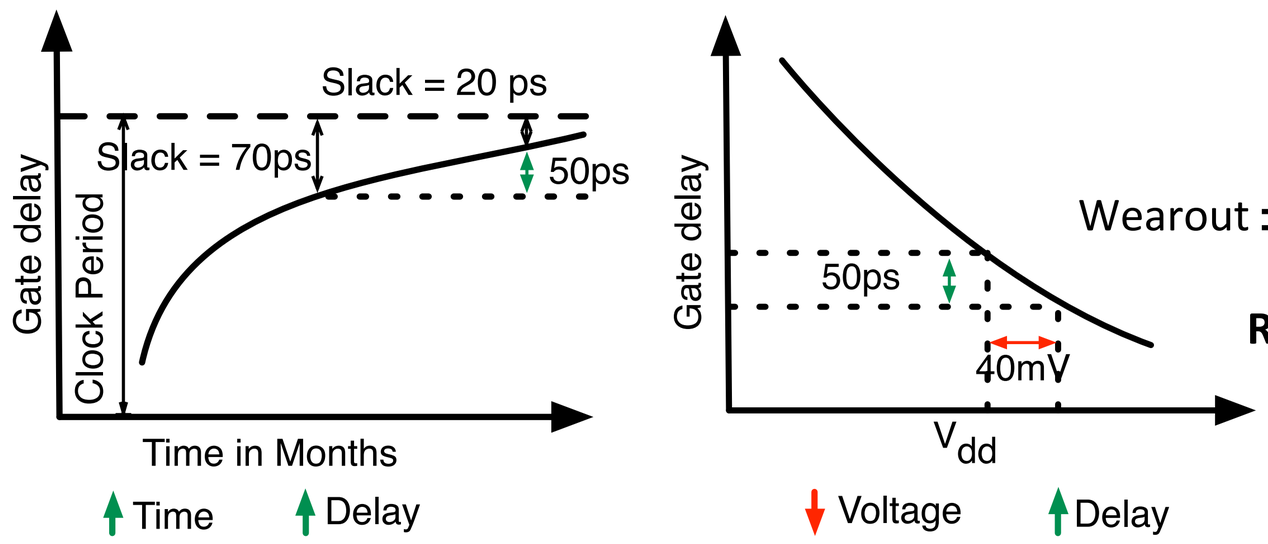
Objective



Average lifetime of microprocessors is expected to decrease ⇒ More failures on the field.

Can we predict the failure?

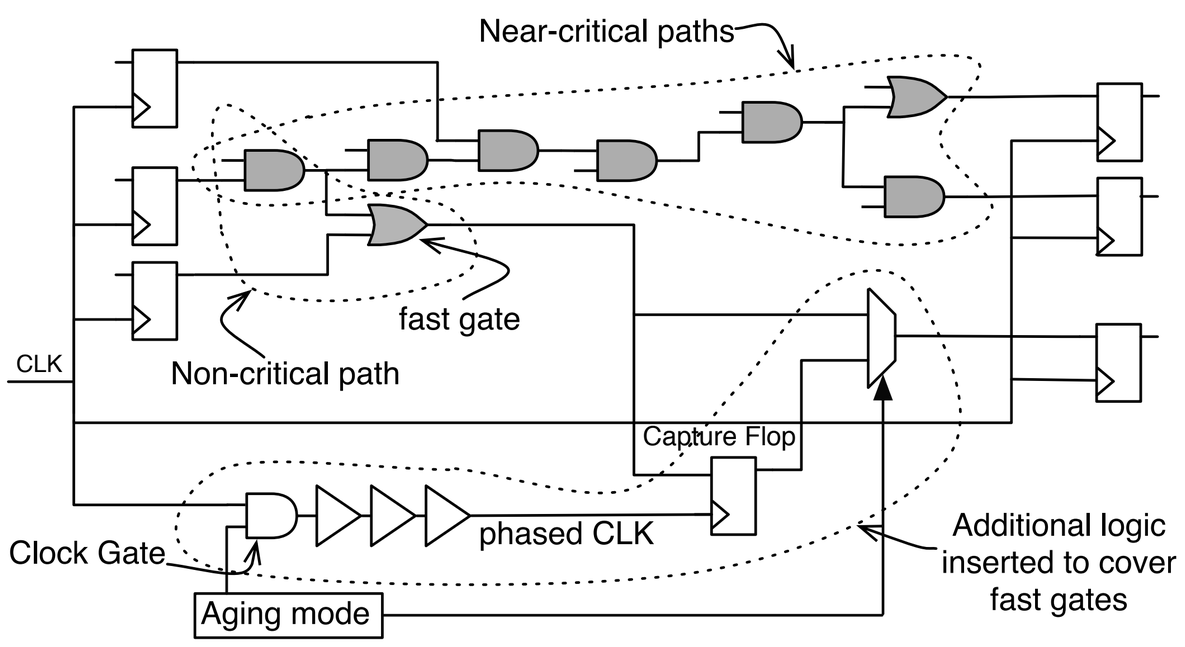
Virtual Aging



Wearout ⇒ delay degrades ⇒ slack decreases

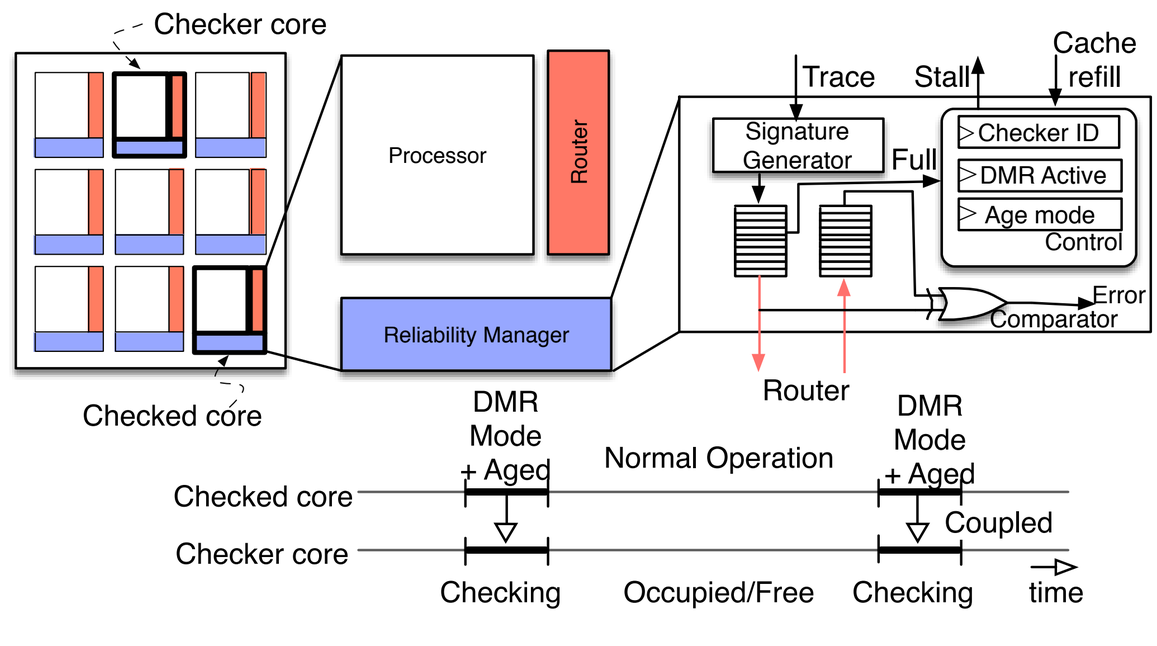
Reducing V_{dd} has the same effect

Delay Degradation ➔ Exposing Failure



- Wearout in critical paths
  - ✓ Naturally exposed
- Wearout in non-critical paths
  - ✓ Clock phase shifting logic

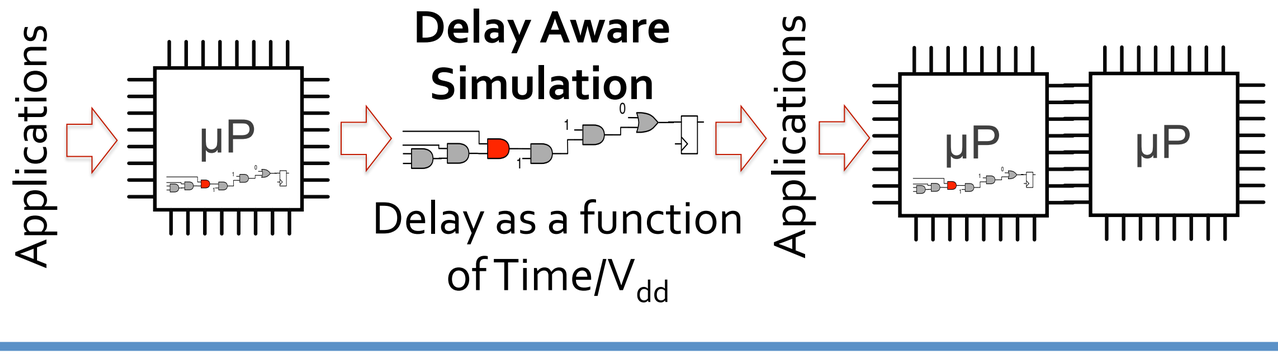
Failure ➔ Detection



Sampling DMR

- Less than 1% energy overhead
- No performance overhead
- 100% Coverage

Evaluation



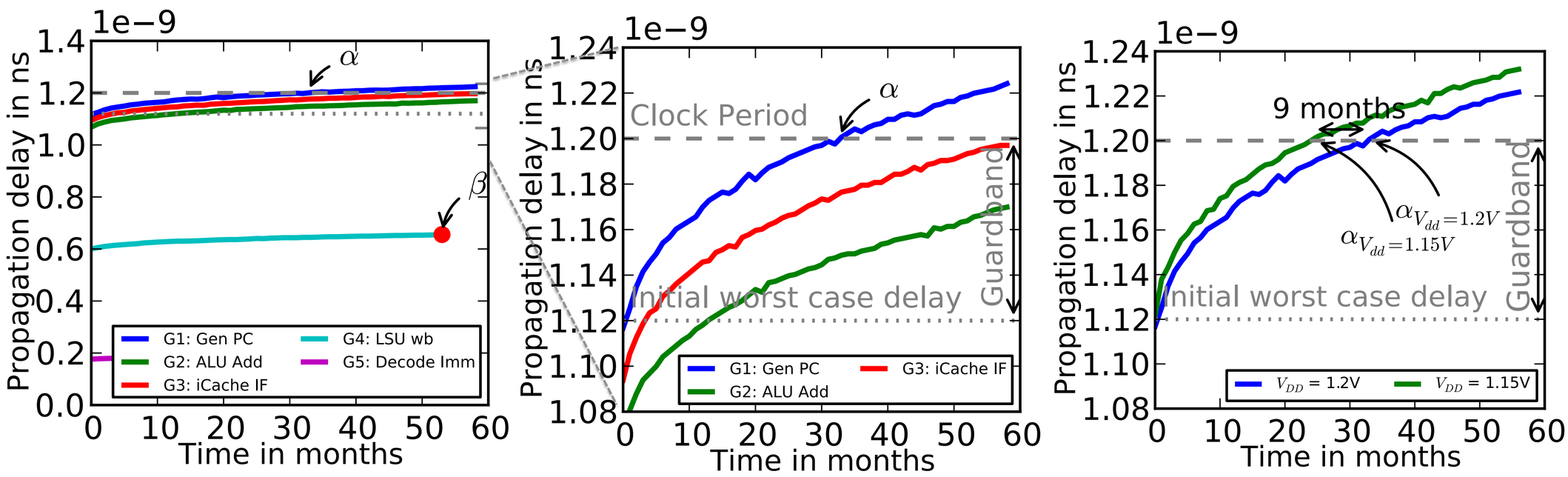
FPGA acceleration

- Full system OpenRISC processor
- Applications – SPEC benchmarks

Synopsys MOSRA

- Wearout model @ transistor level

Results



Delay degradation with wearout

Reducing V_{dd} has a similar effect

50mV reduction in V_{dd} to predict failures 9 months in advance