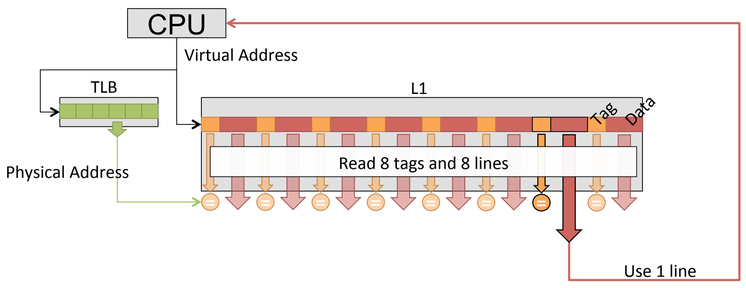
TLC: A Tag-less Cache Design for Reducing Dynamic First Level Cache Energy

UPMARC
Uppsala Programming for Multicore Architectures Research Center

Andreas Sembrant, Erik Hagersten, David Black-Schaffer

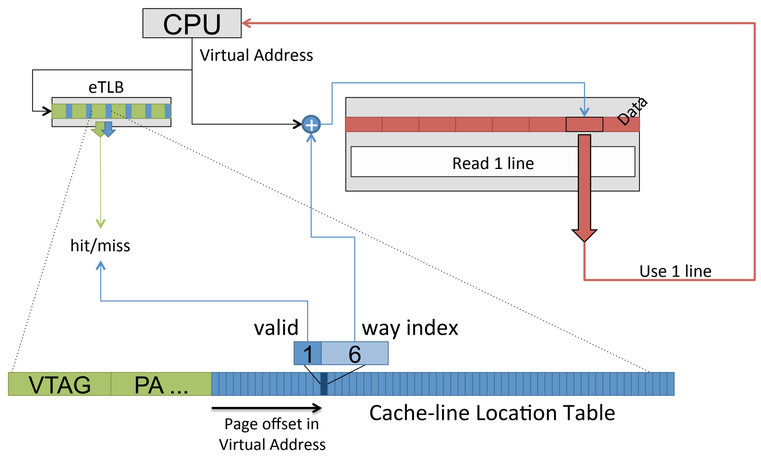
UPPSALA UNIVERSITET

1. Motivation: Standard L1 Cache



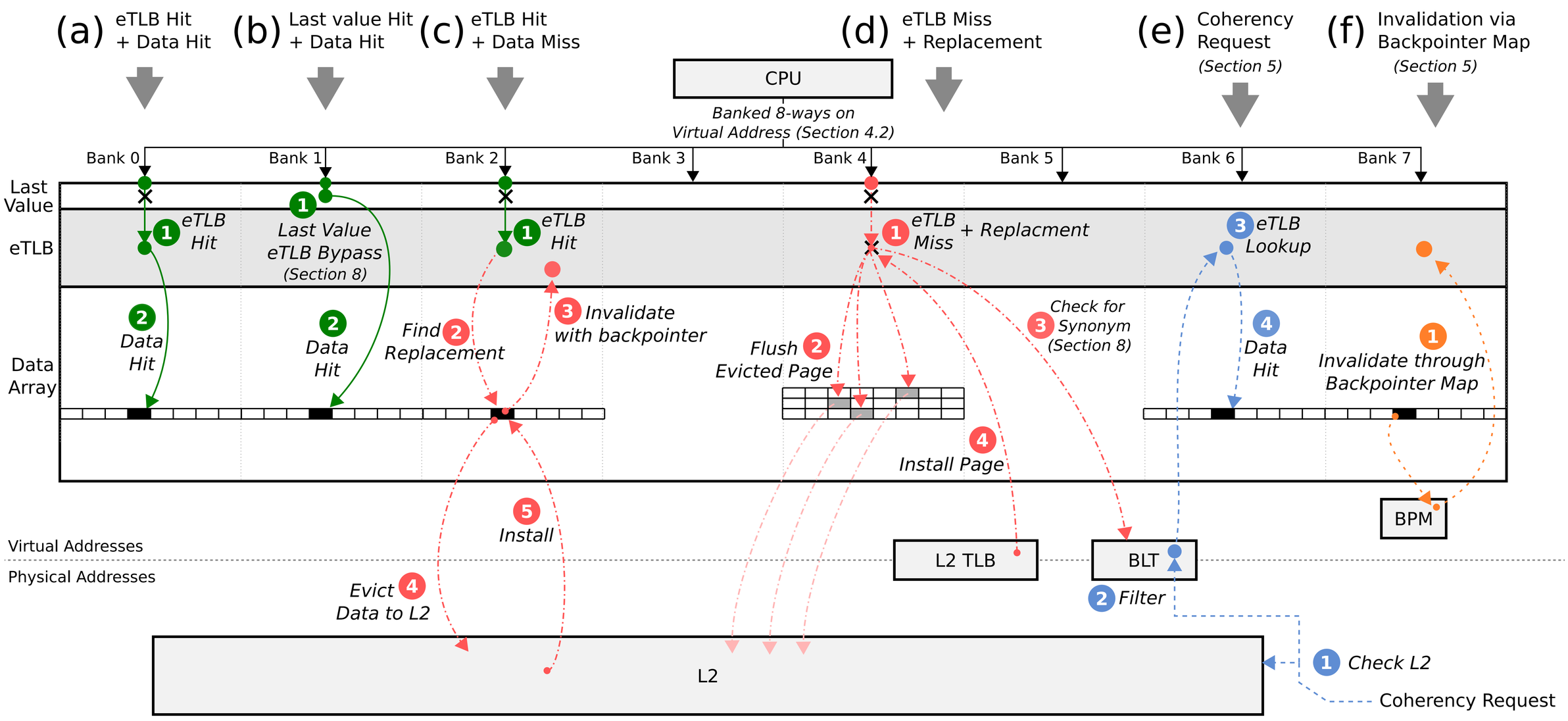
Wastes energy by reading 8 tags and 8 cache lines in parallel when only one cache line is needed.

2. Extended TLB with cache line way information



1. Eliminate extra data-array reads
   by determining the correct correct way from the TLB
2. Eliminate the tag-array
   by avoiding tag comparisions
3. Filter out cache misses
   by checking in the eTLB
4. Better SRAM Shape
   by only reading the correct way
5. Amortize the TLB lookup energy
   by integrating it with way information

3. Overview



4. Optimizations

eTLB Replacement
Minimize forced cache line evictions due to eTLB replacement by evicting the page with least data.

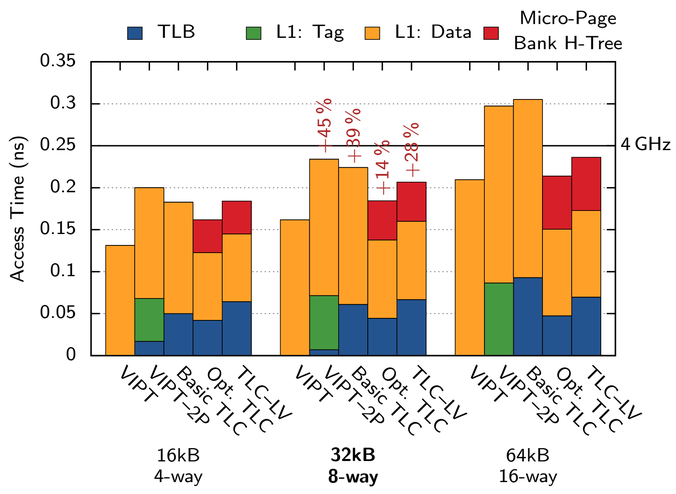
uPages (Sparse Data)
Minimize area when increasing number of eTLB entries by using smaller pages (e.g. 1kB pages)

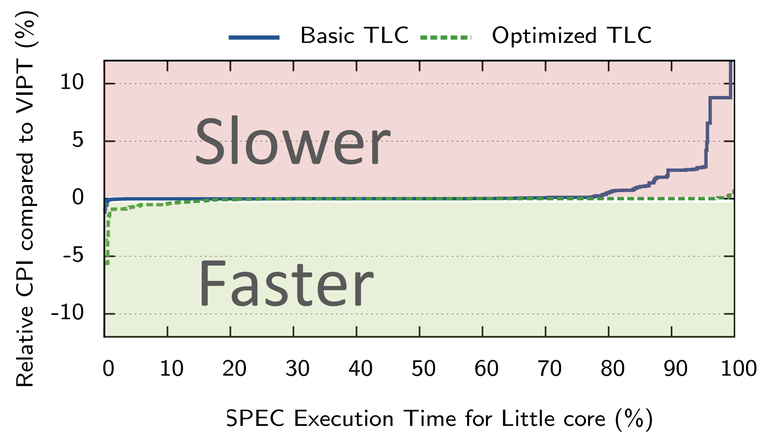
uPage Banking
Optimize eTLB => Data-array communication by banking the eTLB and the data-array on the same uPages.

Last-value eTLB prediction
Bypass eTLB on hits to save eTLB energy.

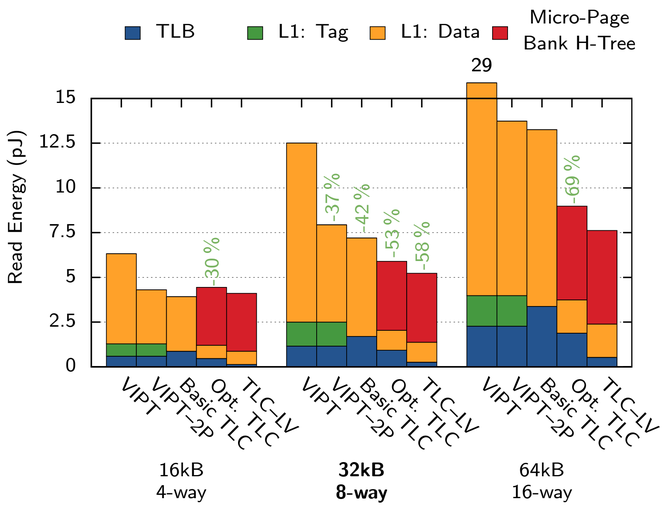
5. Results

Performance





Energy



-78%