39th International Symposium on Microarchitecture Workshop and Tutorial Programs

Walt Disney World Swan Hotel, Orlando, Florida

SATURDAY, DECEMBER 9, 2006

SATURDAY TUTORIALS

Tutorial on
3D Integration for (Micro)Architects
Gabriel Loh (Georgia Tech.), Yuan Xie (Penn. State)

Afternoon Session, 1:30-5pm – Mockingbird1

SATURDAY WORKSHOPS

The 2nd JILP Championship Branch Prediction Competition (CBP-2)
Daniel A. Jiménez (Rutgers)

Morning Session, 8:30am-Noon – Mockingbird1
Noon-1:30pm: Lunch (on your own)

8:30-8:40am: Opening Remarks
8:40-10am: SESSION 1: REALISTIC TRACK
A 256 Kbits L-TAGE Branch Predictor. Andre Seznec (IRISA/INRIA/HIPEAC)
Path Traced Perceptron Branch Predictor Using Local History for Weight Selection. Yasuyuki Ninomiya, Koki Abe (The University of Electro-Communications, Tokyo)
Fused Two-Level Branch Prediction with Ahead Calculation. Yasuo Ishii (NEC)
Selection of the winner of the Realistic Track
10-10:30am: Break (Toucan Foyer)
10:30am-Noon: SESSION 2: IDEALISTIC TRACK
PMPM: Prediction by combining Multiple Partial Matches. Hongliang Gao, Huiyang Zhou (University of Central Florida)
Looking for Limits in Branch Prediction with the GTL Predictor. Andre Seznec (IRISA/INRIA/HIPEAC)
Neuro-PPM Branch Prediction. Ram Srinivasan, Eitan Frachtenberg, Scott Pakin, Olaf Lubeck, Jeanine Cook (Los Alamos National Lab)
Selection of the winner of the Idealistic Track and Future Directions

Workshop on Functionality of Hardware Performance Monitors (FHPM)
Olaf Lubeck (Los Alamos), Rob Fowler (RENCI/UNC), Mike Lang (Los Alamos), Phil Mucci (U. of Tennessee)

Morning & Afternoon Sessions, 8am-6pm – Pelican1

8 -8:30am: Poster Setup
8:30-8:45am: Welcome and Introduction
8:45-10am: SESSION 1
HPM Futures and Visions. Jim Callister (Intel)
GPU Performance Analysis: A Developer's Perspective. Jeffery Keil (Nvidia)
10-10:30am: Break and Posters (Toucan Foyer)
10:30am-Noon: SESSION 2
Designing a HPM from Scratch - A Thousand Events, Please. Wilson Snyder, Phil Mucci (SiCortex)
Enhancing Operating System Algorithms through Hardware Performance Monitoring. Reza Azimi (University of Toronto)
Dynamic Program Stirring on Multiple Cores: How Hardware Performance Monitors Can Help Regulate Performance, Power, and Temperature Simultaneously. Matthew Curtis-Maury (Virginia Tech)
Noon-1:30pm: Lunch (on your own)
1:30-3pm: SESSION 3
Power Update, Cell HPM and What's Hard About Multi-threading. Alex Mericas (IBM)
3-3:30pm: Break and Posters (Toucan Foyer)
3:30-6pm: SESSION 4
Infiniband HPM, Futures and Visions. Michael Kagan (Mellanox)
Design of Xeon/Core 2/Duo HPM, Futures and Visions. Peggy Ireland (Intel)
Performance Monitoring Features in AMD Barcelona. Dave Christie, Anoop Iyer (AMD)
Challenges to a Standard Monitoring Interface. Stephane Eranian (HP)
Tool Infrastructure for Hardware Performance Counters. Adam Leko (University of Florida)

SUNDAY, DECEMBER 10, 2006

SUNDAY TUTORIALS

Tutorial on
Quantum Computing for Architects
Frederic T. Chong (UCSB), Tzvetan S. Metodi (UC Davis), Darshan D. Thaker (UC Davis), Andrew W. Cross (MIT)

Morning Session, 8:30am-Noon – Mockingbird2
Noon-1:30pm: Lunch (on your own)

Tutorial on
The Blue Gene/L Supercomputer: A Hardware and Software Story
Valentina Salapura, IBM T.J. Watson Research Center
Jose E. Moreira, IBM Systems and Technology Group

Afternoon Session, 1:30-5pm – Mockingbird2

SUNDAY WORKSHOPS

Workshop on Design, Architecture and Simulation of Chip Multi-Processors (dasCMP 2006)
Norman Jouppi (HP), Rakesh Kumar (UIUC), Dean Tullsen (UCSD)

Morning & Afternoon Sessions, 8:30am-5pm – Pelican2

8:30-8:45am: Welcome Remarks
8:45-9:30am: Keynote Presentation
Opportunities and Challenges of the 1000-thread CMP. Jim Laudon (Sun)
9:30-10am: SESSION 1
Providing Hardware Support for Software Controlled Multithreading. Aqeel Mahesri, Nicholas J. Wang, Sanjay J. Patel (UIUC)
10-10:30am: Break (Toucan Foyer)
10:30am-Noon: SESSION 2: CACHE AND BANDWIDTH ISSUES
CMP Cache Performance Projection: Accessibility vs. Capacity. Xudong Shi, Feiqi Su, Jih-kwon Peir, Ye Xia, Zhen Yang (UFl)
From Chaos to QoS: Case Studies in CMP Resource Management. Hari Kannan (Stanford), Fei Guo (NC State), Li Zhao (Intel), Ramesh Illikkal (Intel), Ravi Iyer (Intel), Don Newell (Intel), Yan Solihin (NC State), Christos Kozyrakis (Stanford)
Improving Fairness, Throughput and Energy-Efficiency on a Chip Multiprocessor through DVFS. Masaaki Kondo, Hiroshi Sasaki, Hiroshi Nakamura (Univ of Tokyo)
Noon-1:30pm: Lunch (on your own)
1:30-3pm: SESSION 3: EXPLOITING AND EXPRESSING PARALLELISM
Starvation-Free Commit Arbitration Policies for Transactional Memory Systems. M.M. Waliullah, Per Stenstrom (Chalmers)
An hardware/software framework for supporting Transactional Memory in a MPSoC environment. Cesare Ferri1 (Brown), Tali Moreshet (Swarthmore), R.Iris Bahar (Brown), Luca Benini (Bologna), and Maurice Herlihy (Brown)
Function Level Parallelism Driven by Data Dependencies. Sean Rul, Hans Vandierendonck, Koen De Bosschere (Ghent)
3-3:30pm: Break (Toucan Foyer)
3:30-5pm: SESSION 4: PANEL DISCUSSION
Top CMP Research Problems: An Industrial Perspective
Participants: Konrad Lai (Intel), David Christie (AMD), Pradip Bose (IBM), Jim Laudon (Sun), Norman Jouppi (HP)

2nd Workshop on Architectural Reliability (WAR-2)
Oğuz Ergin (TOBB University of Economics and Technology), Osman Unsal (Barcelona Supercomputing Center)

Morning Session, 8:30am-Noon – Mockingbird1
Noon-1:30pm: Lunch (on your own)

8:30-10am: SESSION 1
Non-Uniform Fault Tolerance. Jonathan Chang, George A. Reis, Neil Vachharajani, Ram Rangan, David I. August (Princeton)
Configurable Transient Fault Detection via Dynamic Binary Translation. George A. Reis, Jonathan Chang, David I. August, Robert Cohn, Shubhendu S. Mukherjee (Princeton, Intel)
Exploiting Eager Register Release in a Redundantly Multi-Threaded Processor. Niti Madan, Rajeev Balasubramonian (University of Utah)
10-10:30am: Break (Toucan Foyer)
10:30am-Noon: SESSION 2
Locality-Based Information Redundancy for Processor Reliability. Martin Dimitrov, Huiyang Zhou (Univeristy of Central Florida)
Online Timing Analysis for Wearout Detection. Jason A. Blome, Shuguang Feng, Shantanu Gupta, Scott Mahlke (University of Michigan)
Quantifying the Impact of Process Variability on Microprocessor Behavior. Bogdan F. Romanescu, Sule Ozev, Daniel J. Sorin (Duke)

Reconfigurable and Adaptive Architecture Workshop (RAAW)
Aneesh Aggarwal (SUNY Binghamton), Pradip Bose (IBM T. J. Watson), Mohamed Zahran (CUNY)

Afternoon Session, 1:30-5pm – Mockingbird1

1:30-3pm: SESSION 1
Keynote Speech: Prof. David Albonesi, Cornell University
Adaptive Multi-threaded Microprocessors
Mapping Streaming Architectures on Reconfigurable Platforms. Nikolaos Bellas, Sek M. Chai, Malcolm Dwyer, Dan Linzmeier (Embedded Systems Research, Motorola Labs)
3-3:30pm: Break (Toucan Foyer)
3:30-5pm: SESSION 2
Custom Code Generation for Soft Processors. Martin Labrecque, Peter Yiannacouras, J. Gregory Steffan (University of Toronto)
Improving Instruction Level Parallelism through Reconfigurable Units in Superscalar Processors. Tameesh Suri (SUNY at Binghamton)
Architectural Contesting: Exposing and Exploiting Temperamental Behavior. Hashem H. Najaf-abadi, Eric Rotenberg (NC State University)