39th International Symposium on Microarchitecture
Main Technical Program
Walt Disney World Swan Hotel, Orlando, Florida

SUNDAY, DECEMBER 10, 2006

6-9pm: Reception Dinner (Swan 7-10)

MONDAY, DECEMBER 11, 2006

7am: Continental Breakfast (Osprey Ballroom)
8:15-8:30am: Opening Remarks (Swan 7-10)
8:30-9:30am: Keynote I (Swan 7-10, Chair: Scott Mahlke, Michigan)
Wen-mei Hwu, U. of Illinois
Top five reasons why sequential programming models could be the best way to program many-core systems
9:30-10am: Break (Swan Foyer 10)
10am-Noon: SESSION 1: RELIABILITY AND BUG DETECTION
(Swan 7-10, Chair: Pradip Bose, IBM)
A Floorplan-Aware Dynamic Inductive Noise Controller for Reliable Processor Design. Fayez Mohamood, Michael Healy, Sung Kyu Lim, Hsien-Hsin S. Lee (Georgia Tech.)
Yield-Aware Cache Architectures. Serkan Ozdemir, Debjit Sinha, Gokhan Memik, Jonathan Adams, Hai Zhou (Northwestern)
Phoenix: Detecting and Recovering from Permanent Processor Design Bugs with Programmable Hardware. Smruti Sarangi, Abhishek Tiwari, Josep Torrellas (U. Illinois)
PathExpander: Architectural Support for Increasing the Path Coverage of Dynamic Bug Detection. Shan Lu, Pin Zhou, Wei Liu, Yuanyuan Zhou, Josep Torrellas (U. Illinois)
Noon-1:30pm: Lunch (Osprey Ballroom)
1:30-3:30pm: SESSION 2A: COMPILER AND BRANCH HANDLING
(Swan 7&8, Chair: Craig Zilles, U. Illinois)
Diverge-Merge Processor (DMP): Dynamic Predicated Execution of Complex Control-Flow Graphs Based on Frequently Executed Paths. Hyesoon Kim†, Jose A. Joao†, Onur Mutlu‡, Yale N. Patt† (†UT-Austin, ‡Microsoft Research)
Head and Tail Duplication for Convergent Hyperblock Formation. Bertrand A. Maher, Aaron Smith, Doug Burger, Kathryn McKinley (UT-Austin)
Data-Dependency Graph Transformations for Superblock Scheduling. Mark Heffernan, Kent Wilken, Ghassan Shobaki (UC-Davis)
Dataflow Predication. Aaron Smith, Doug Burger, Steve Keckler, Kathryn McKinley, Ramdas Nagarajan, Karu Sankaralingam, Robert McDonald (UT-Austin)
1:30-3:30pm: SESSION 2B: SECURITY
(Swan 9&10, Chair: David August, Princeton)
Authentication Control Point and its Implications for Secure Processor Design. Weidong Shi (Motorola), Hsien-Hsin S. Lee (Georgia Tech.)
Using Branch Correlation to Identify Infeasible Paths for Anomaly Detection. Xiaotong Zhuang, Tao Zhang, Santosh Pande (Georgia Tech.)
Memory Protection through Dynamic Access Control. Kun Zhang, Tao Zhang, Santosh Pande (Georgia Tech.)
LIFT: A Low-Overhead Practical Information Flow Tracking System for Detecting General Security Attacks. Feng Qin‡, Zhenmin Li†, Yuanyuan Zhou†, Cheng Wang*, Ho-seop Kim*, Youfeng Wu* (‡Ohio State, †U. Illinois, *Intel Research)
3:30-4pm: Break (Swan Foyer 10)
4-5:30pm: SESSION 3A: SUPERSCALAR PROCESSORS
(Swan 7&8, Chair: Gabriel Loh, Georgia Tech)
Fairness and Throughput in Switch on Event Multithreading. Ron Gabor†, Shlomo Weiss†, Avi Mendelson‡ (†Tel-Aviv University, ‡Intel)
A Predictive Performance Model for Superscalar Processors. P. J. Joseph‡, Kapil Vaswani†, Matthew J. Thazhuthaveetil† (‡Freescale, †Indian Institute of Science)
Serialization-Aware Mini-Graphs: Performance with Fewer Resources. Anne Bracy†‡, Amir Roth† (†U. Penn., ‡Intel)
4-5:30pm: SESSION 3B: MEMORY SYSTEMS
(Swan 9&10, Chair: Russ Joseph, Northwestern)
Architectural Support for Software Transactional Memory. Bratin Saha, Ali-Reza Adl-Tabatabai, Quinn Jacobson (Intel)
Virtually Pipelined Network Memory. Banit Agrawal, Timothy Sherwood (UC-Santa Barbara)
Fair Queuing CMP Memory Systems. Kyle J. Nesbit†, Nidhi Aggarwal†, James Laudon‡, James E. Smith† (†UW-Madison, ‡Sun)
5:30-6pm: Break (Swan Foyer 10)
6-7:30pm: PANEL SESSION (Swan 7-10)
Nanotechnology's Role in Shaping Future Architectures
Alvin R. Lebeck (Chair/Moderator), Doug Burger, Chris Dwyer, Michael Niemier, Yale Patt
10-11:30pm: Business Meeting (Swan 7-10)

TUESDAY, DECEMBER 12, 2006

7am: Continental Breakfast (Osprey Ballroom)
8-9am: Keynote II (Swan 7-10, Chair: Bill Mangione-Smith, QIPS)
Sanjay J. Patel, U. of Illinois and AGEIA Technologies
Attack of the Killer Game Machines
9-9:30am: Break (Swan Foyer 10)
9:30-11:30am: SESSION 4: CMP EXECUTION
(Swan 7-10, Chair: John Shen, Nokia)
Reunion: Complexity-Effective Multicore Redundancy. Jared C. Smolens, Brian T. Gold, Babak Falsafi, James C. Hoe (Carnegie Mellon)
Exploiting Fine-Grained Data Parallelism with Chip Multiprocessors and Fast Barriers. Jack Sampson†, Ruben Gonzalez*, Jean-Francois Collard**, Norman P. Jouppi**, Mike Schlansker**, Brad Calder†‡ (†UC-San Diego, *UPC Barcelona, **HP Labs, ‡Microsoft)
CAPSULE: Hardware-Assisted Parallel Execution of Component-Based Programs. Pierre Palatin, Yves Lhuillier, Olivier Temam (INRIA)
Support for High-Frequency Streaming in CMPs. Ram Rangan†, Neil Vachharajani†, Adam Stoler†, Guilherme Ottoni†, David August†, George Cai‡ (†Princeton, ‡Intel)
11:30am-1pm: Lunch (Osprey Ballroom)
1-2:30pm: SESSION 5A: MEMORY DEPENDENCES
(Swan 7&8, Chair: Antonio Gonzalez, UPC and Intel)
Fire-and-Forget: Load/Store Scheduling with No Store Queue at All. Samantika Subramaniam, Gabriel H. Loh (Georgia Tech.)
NoSQ: Store-Load Communication without a Store Queue. Tingting Sha, Milo M. K. Martin, Amir Roth (U. Penn.)
DMDC: Delayed Memory Dependence Checking through Age-based Filtering. Fernando Castro†, Daniel Chaver†, Luis Pinuel†, Manuel Prieto†, Michael C. Huang‡, Francisco Tirado† (†University Complutense of Madrid, ‡U. Rochester)
1-2:30pm: SESSION 5B: NETWORKS AND COHERENCE
(Swan 9&10, Chair: Steve Keckler, UT-Austin)
Coherence Ordering for Ring-based Chip Multiprocessors. Michael R. Marty, Mark D. Hill (UW-Madison)
In-Network Cache Coherence. Noel Eisley†, Li-Shiuan Peh†, Li Shang‡ (†Princeton, ‡Queens University)
ViChaR: A Dynamic Virtual Channel Regulator for Network-on-Chip Routers. Chrysostomos A. Nicopoulos†, Dongkook Park†, Jongman Kim†, Narayanan Vijaykrishnan†, Mazin S. Yousif‡, Chita R. Das† (†Penn. State, ‡Intel)
2:30-3pm: Break (Swan Foyer 10)
3-4:30pm: SESSION 6A: POWER
(Swan 7&8, Chair: Richard Belgard, Consultant)
An Analysis of Efficient Multi-Core Global Power Management Policies: Maximizing Performance for a Given Power Budget. Canturk Isci†, Alper Buyuktosunoglu‡, Pradip Bose‡, Margaret Martonosi†, Chen-Yong Cher‡ (†Princeton, ‡IBM)
Dynamic Standby Prediction for Leakage Tolerant Microprocessor Functional Units. Ahmed Youssef, Mohab Anis, Mohamed Elmasry (U. Waterloo)
Live, Runtime Phase Monitoring and Prediction on Real Systems with Application to Dynamic Power Management. Canturk Isci, Gilberto Contreras, Margaret Martonosi (Princeton)
3-4:30pm: SESSION 6B: CACHES AND PREFETCHING
(Swan 9&10, Chair: Timothy Sherwood, UC-Santa Barbara)
Adaptive Caches: Effective Shaping of Cache Behavior to Workloads. Ranjith Subramanian, Yannis Smaragdakis, Gabriel H. Loh (Georgia Tech.)
Memory Prefetching Using Adaptive Stream Detection. Ibrahim Hur†‡, Calvin Lin† (†UT-Austin, ‡IBM)
Scalable Cache Miss Handling for High Memory-Level Parallelism. James Tuck, Luis Ceze, Josep Torrellas (U. Illinois)
4:30pm: Banquet/Excursion: Fulton's Crab House, Cirque du Soleil

WEDNESDAY, DECEMBER 13, 2006

7am: Continental Breakfast (Osprey Ballroom)
8-10am: SESSION 7: MANAGING CMP CACHES
(Swan 7-10, Chair: David Albonesi, Cornell)
Utility-Based Cache Partitioning: A Low-Overhead, High-Performance, Runtime Mechanism to Partition Shared Caches. Moinuddin K. Qureshi, Yale N. Patt (UT-Austin)
Molecular Caches: A Caching Structure for Dynamic Creation of Application-Specific Heterogeneous Cache Regions. Keshavan Varadarajan†, S. K. Nandy†, Vishal Sharda†, Amrutur Bharadwaj†, Ravi Iyer‡, Srihari Makineni‡, Donald Newell‡ (†Indian Inst. of Sci., ‡Intel)
ASR: Adaptive Selective Replication for CMP Caches. Bradford M. Beckmann, Michael R. Marty, David A. Wood (UW-Madison)
Managing Distributed, Shared L2 Caches through OS-Level Page Allocation. Sangyeun Cho, Lei Jin (U. of Pittsburgh)
10-10:30am: Break (Swan Foyer 10)
10:30am-12:30pm: SESSION 8: TECHNOLOGY-DRIVEN ARCHITECTURE
(Swan 7-10, Chair: Gokhan Memik, Northwestern)
Die Stacking (3D) Microarchitecture. Bryan Black†, Murali Annavaram†, Ned Brekelbaum†, John DeVale†, Lei Jiang†, Gabriel H. Loh‡, Don McCauley†, Pat Morrow†, Donald W. Nelson†, Daniel Pantuso†, Paul Reed†, Jeff Rupley†, Sadasivan Shankar†, John Shen†, Clair Webb† (†Intel, ‡Georgia Tech.)
Distributed Microarchitectural Protocols in the TRIPS Prototype Processor. Karthikeyan Sankaralingam†, Ramadass Nagarajan†, Robert McDonald†, Rajagopalan Desikan†‡, Saurabh Drolia†*, Madhu Saravana Sibi Govindan†, Paul Gratz†, Divya Gulati†, Heather Hanson†, Changkyu Kim†, Haiming Liu†, Nitya Ranganathan†, Simha Sethmadhavan†, Sadia Sharif†, Premkishore Shivakumar†, Stephen W. Keckler†, Doug Burger† (†UT-Austin, ‡AMD, *Microsoft)
Leveraging Optical Technology in Future Bus-based Chip Multiprocessors. Nevin Kirman, Meyrem Kirman, Rajeev K. Dokania, Jose F. Martinez, Alyssa B. Apsel, Matthew A. Watkins, David H. Albonesi (Cornell)
Mitigating the Impact of Process Variations on CPU Register File and Execution Units. Xiaoyao Liang, David Brooks (Harvard)
12:30-1pm: Closing/Awards (Swan 7-10)