Microarchitecture and Design Challenges for Gigascale Integration

Shekhar Borkar

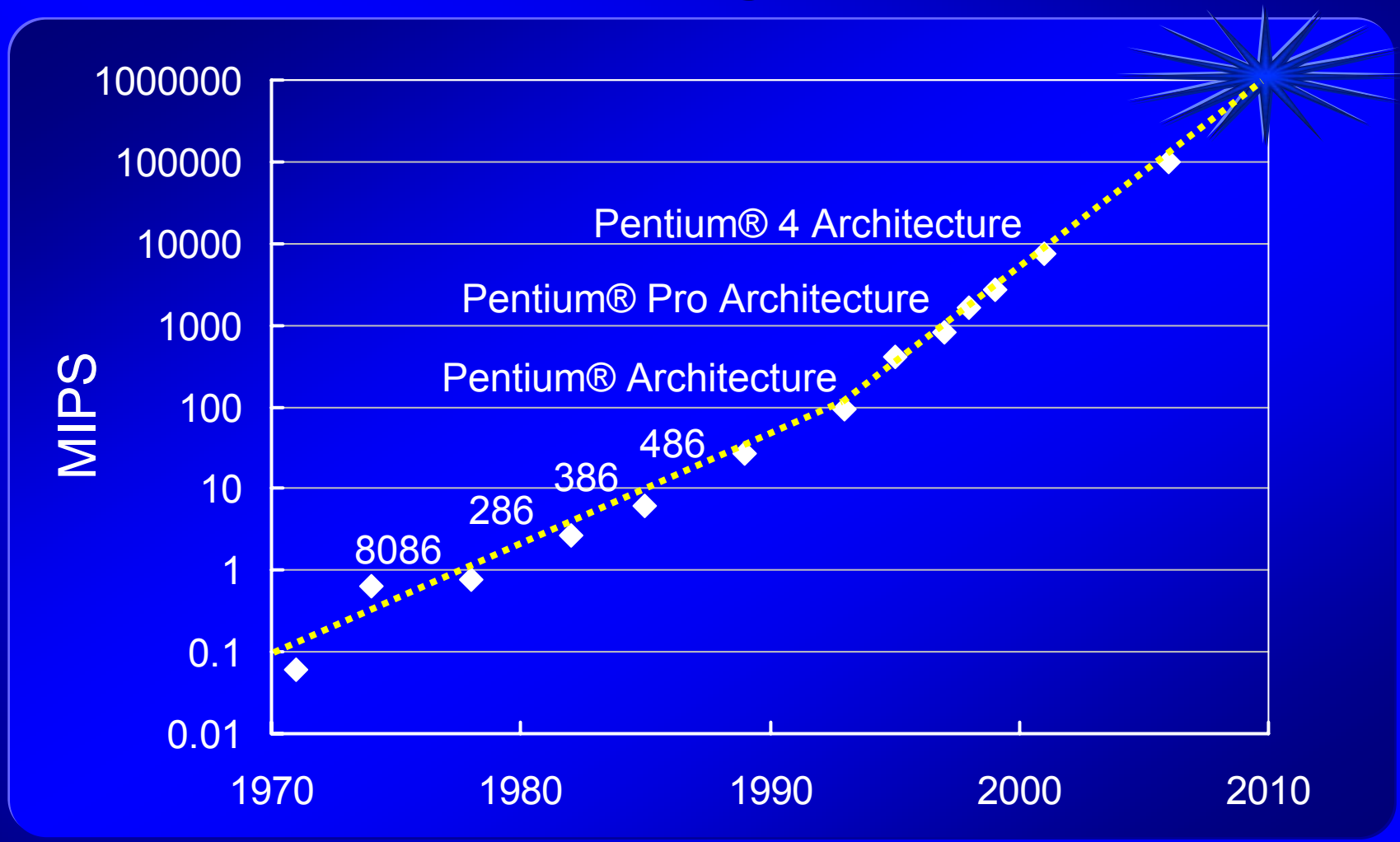
Intel Corp.

December 6, 2004

Outline

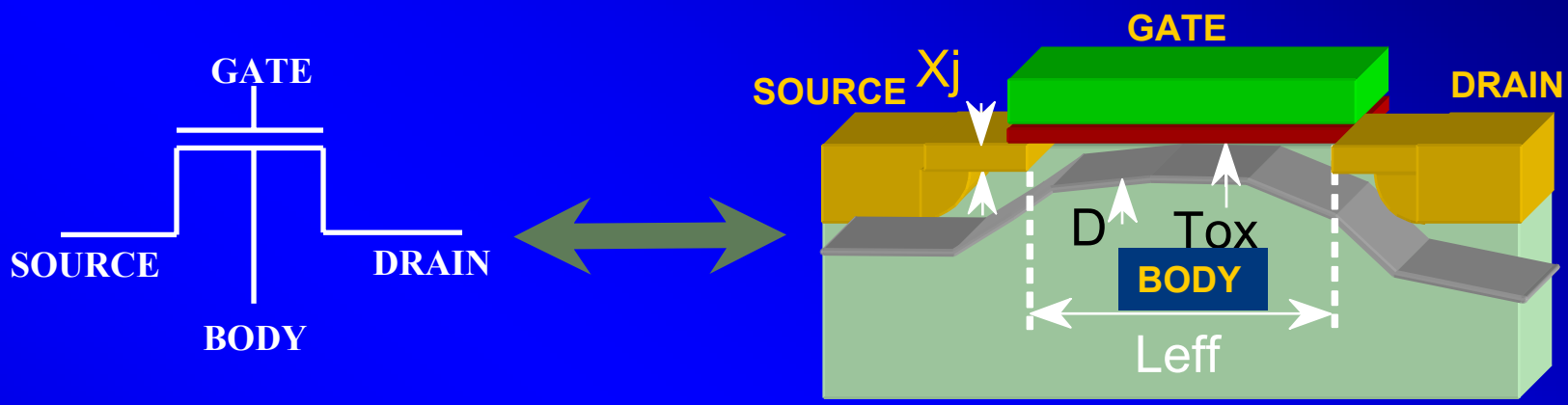
- Process technology scaling & near term challenges
- μArchitecture & Design solutions
- Upcoming paradigm shifts
- Long term outlook & challenges
- Summary

Goal: 1TIPS by 2010



How do you get there?

Technology Scaling



Dimensions scale down by 30%	Doubles transistor density
Oxide thickness scales down	Faster transistor, higher performance
Vdd & Vt scaling	Lower active power

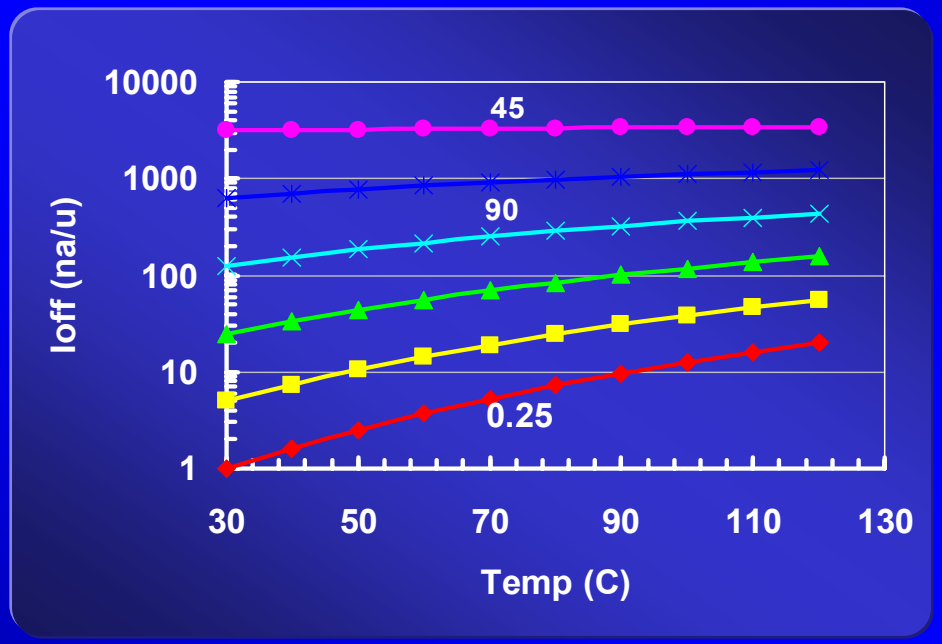
Scaling will continue, but with challenges!

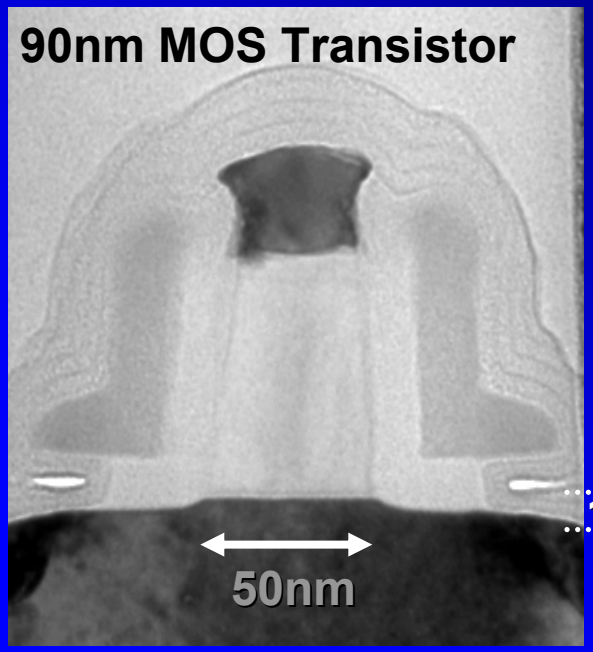
Technology Outlook

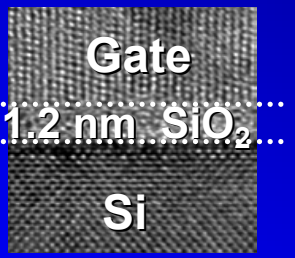
High Volume Manufacturing	2012	2014	2016	2018
Technology Node (nm)	22	16	11	8
Integration Capacity (BT)	32	64	128	256
Delay = CV/I scaling	ay scaling will slow down			
Energy/Logic Op scaling	gy scaling will slow down			
Bulk Planar CMOS	Low Probability			
Alternate, 3G etc	High Probability			
Variability	h Very High			
ILD (K)	ce slowly towards 2-2.5			
RC Delay	1	1	1	1
Metal Layers	to 1 layer per generation			

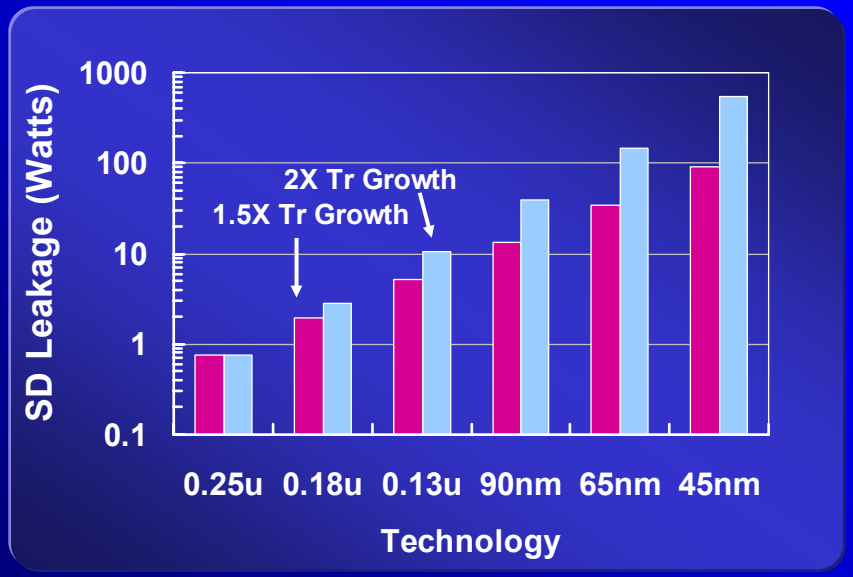

power
&
energy

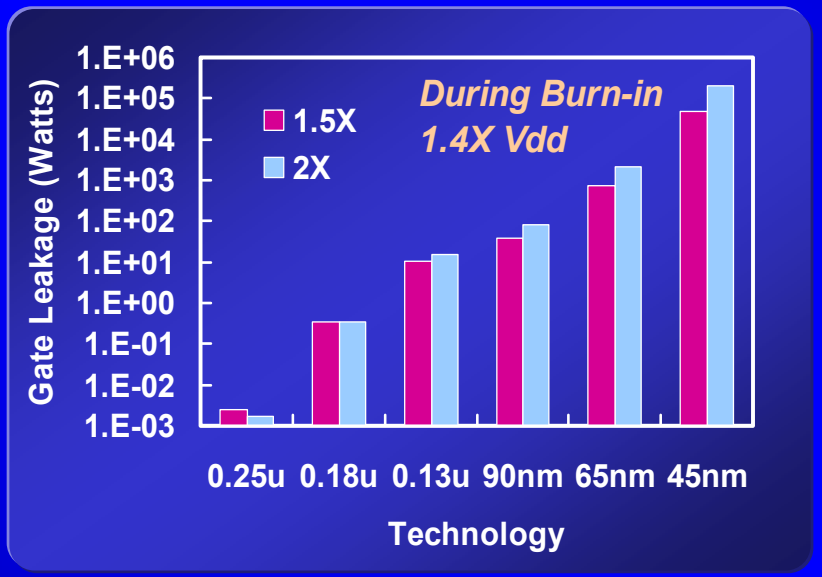
The Leakage(s)...



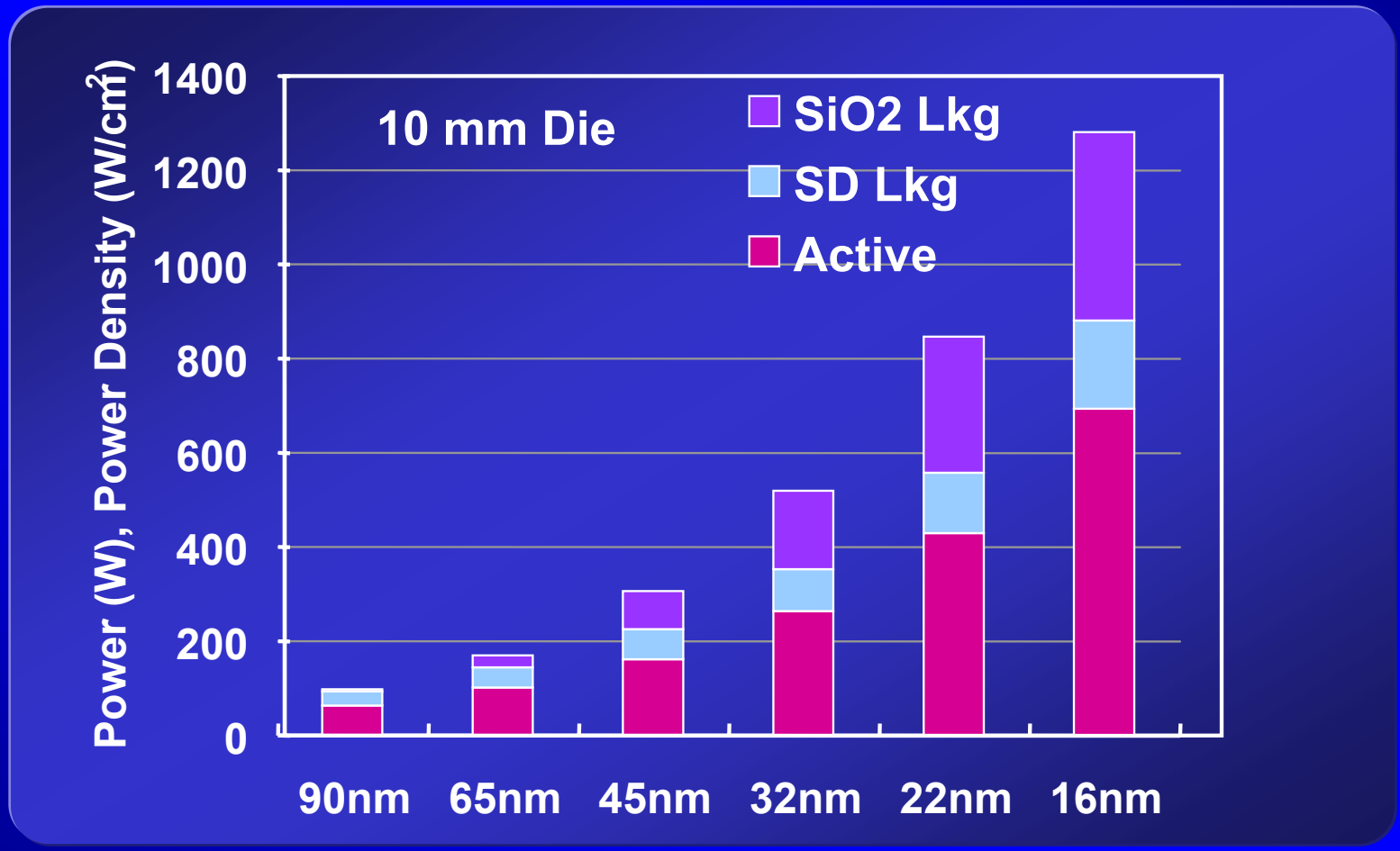






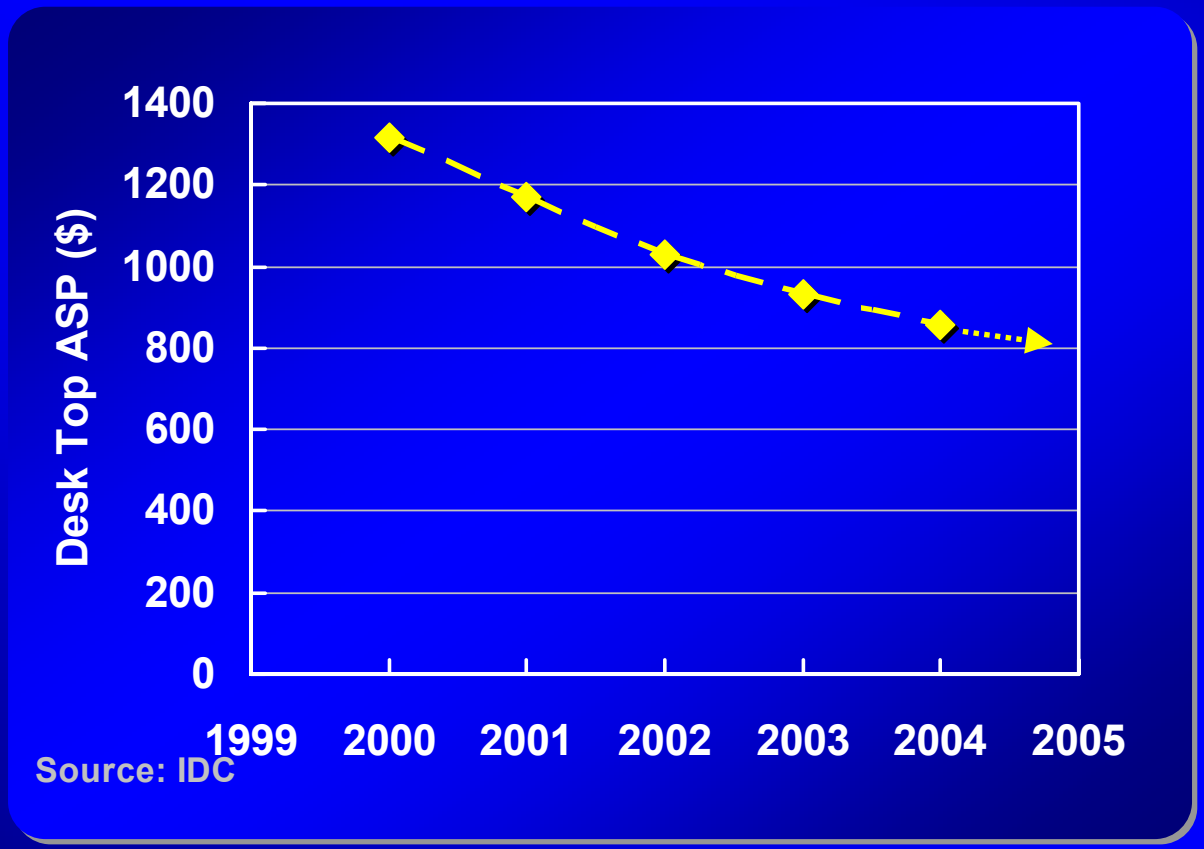


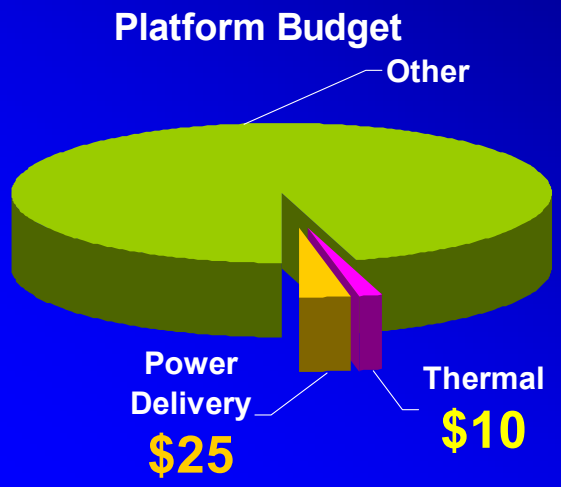
Projected Power (unconstrained)



Active and Leakage power will become prohibitive

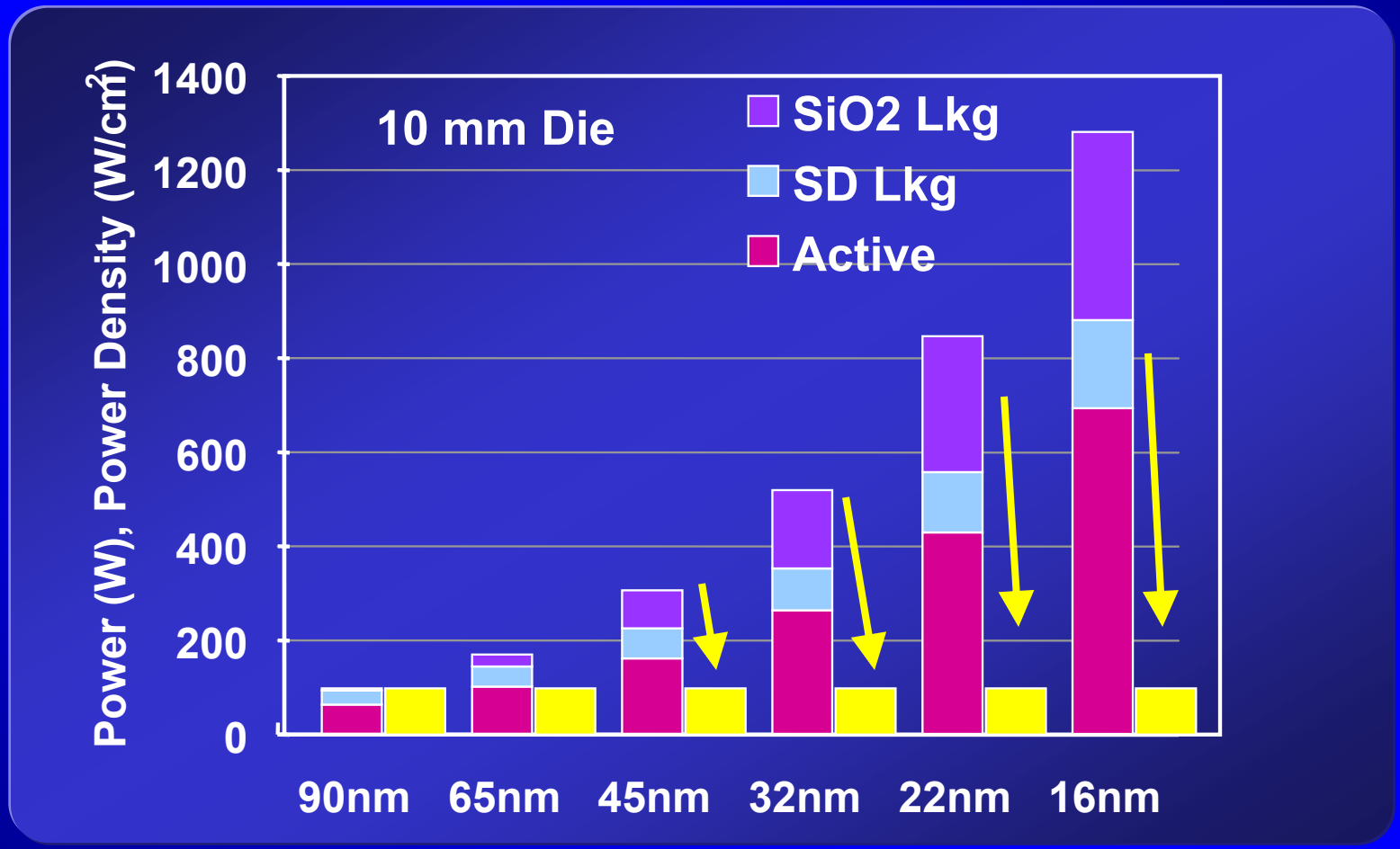
Product Cost Pressure





Shrinking ASP, and shrinking $ budget for power

Must Fit in Power Envelope



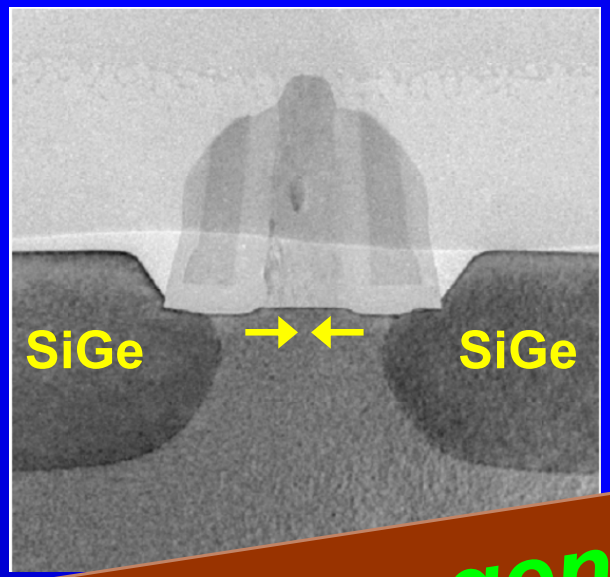
Technology, Circuits, and Architecture to constrain the power

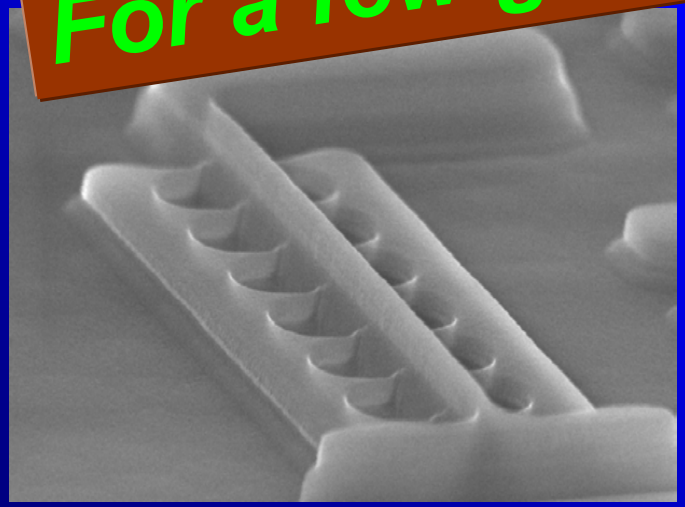
Between Now and Then—

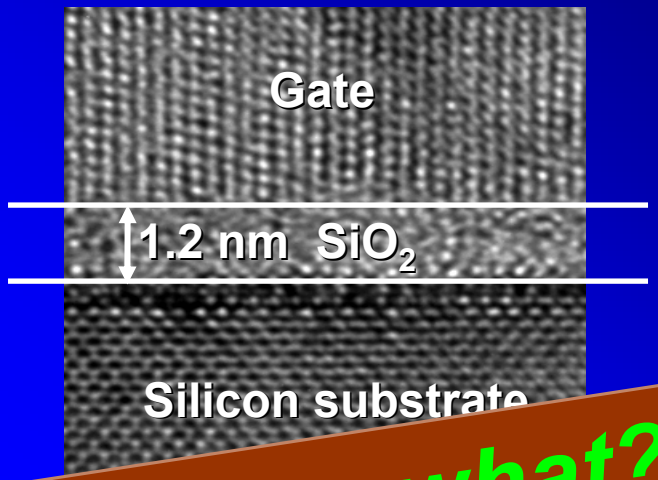
- Move away from Frequency alone to deliver performance
- More on-die memory
- Multi-everywhere
  - Multi-threading
  - Chip level multi-processing
- Throughput oriented designs
- Valued performance by higher level of integration
  - Monolithic & Polylithic

Leakage Solutions

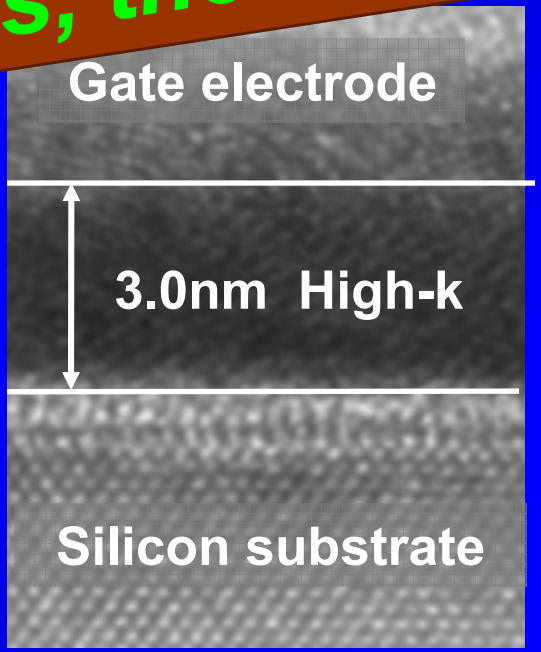
Planar Transistor



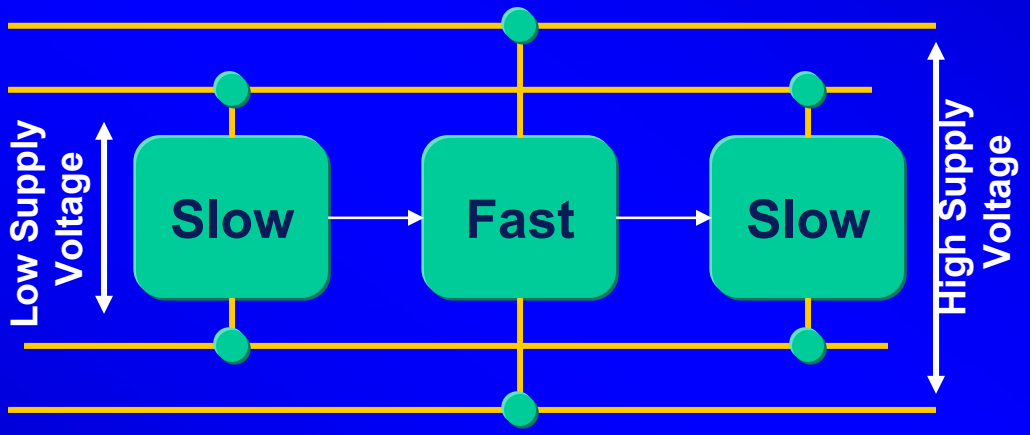




For a few generations, then what?

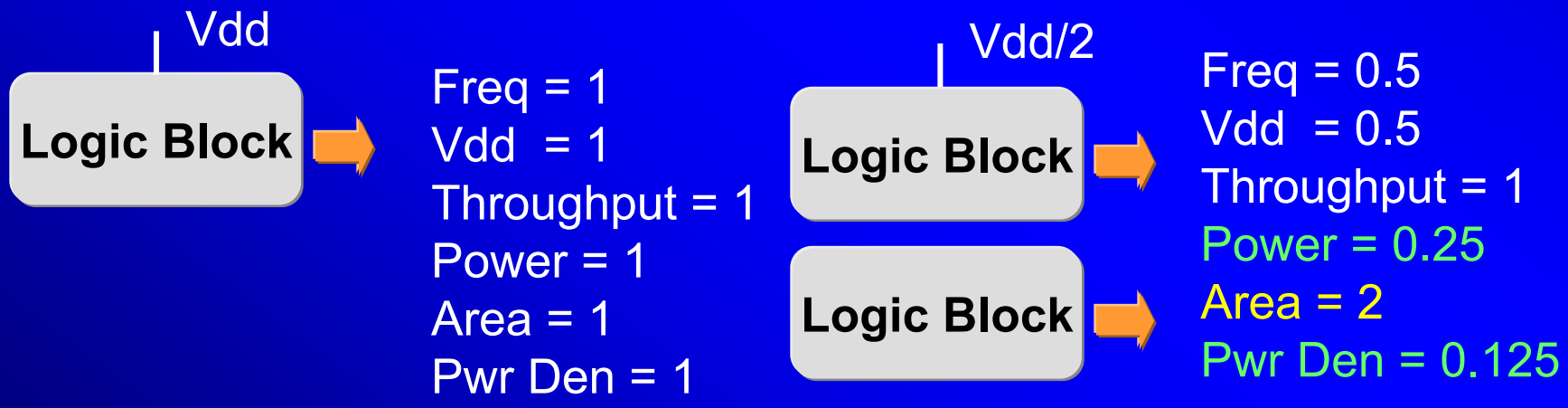


Active Power Reduction

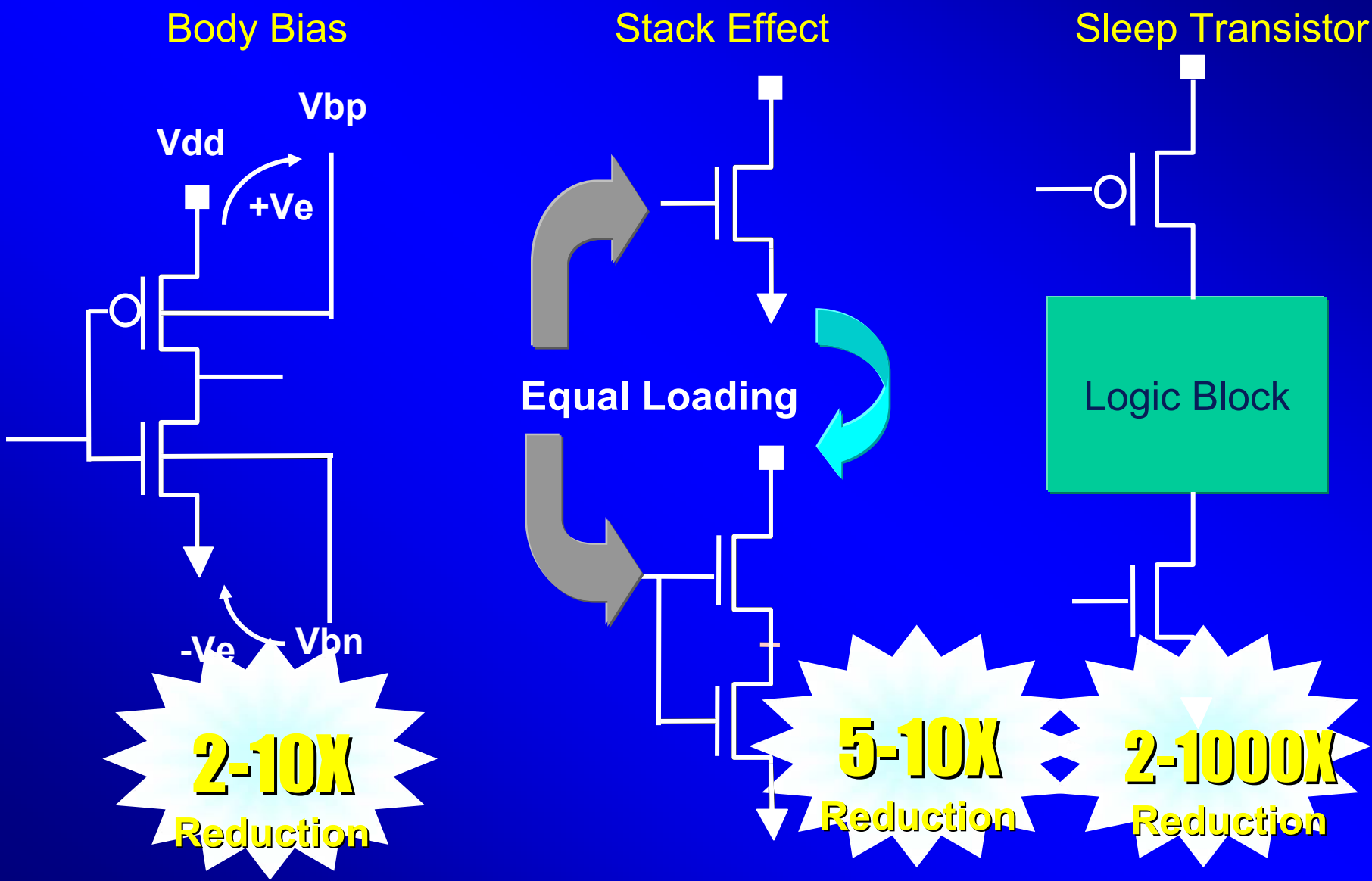


Multiple Supply Voltages

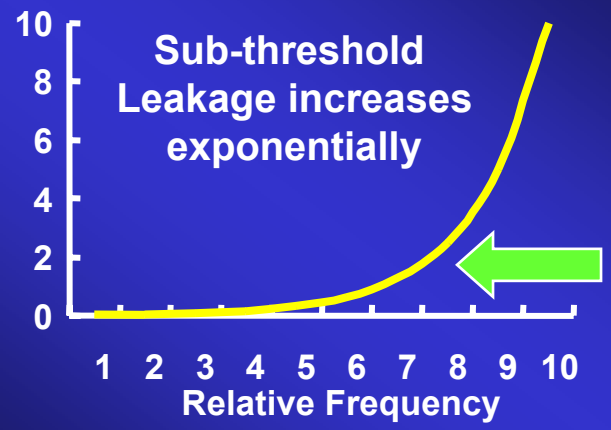
Throughput Oriented Designs



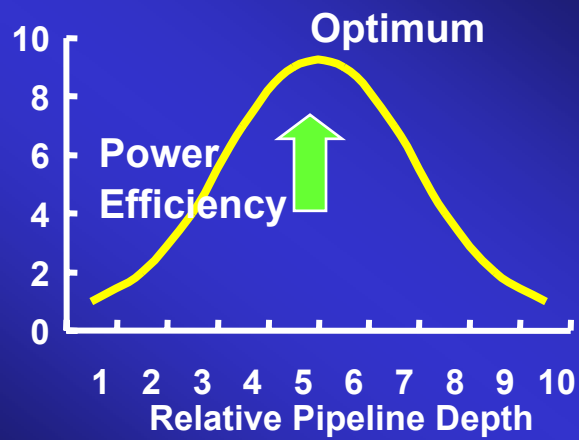
Leakage Control



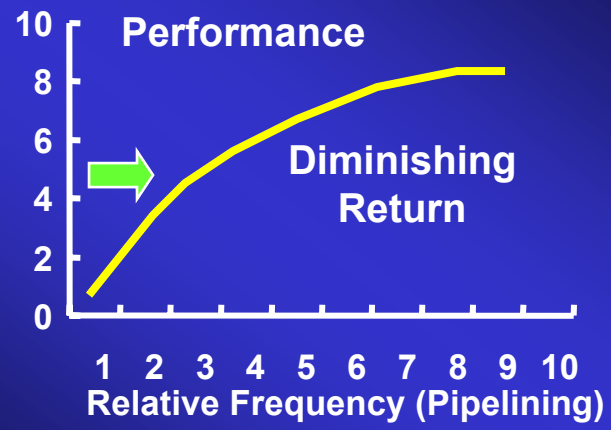
Optimum Frequency



Process Technology



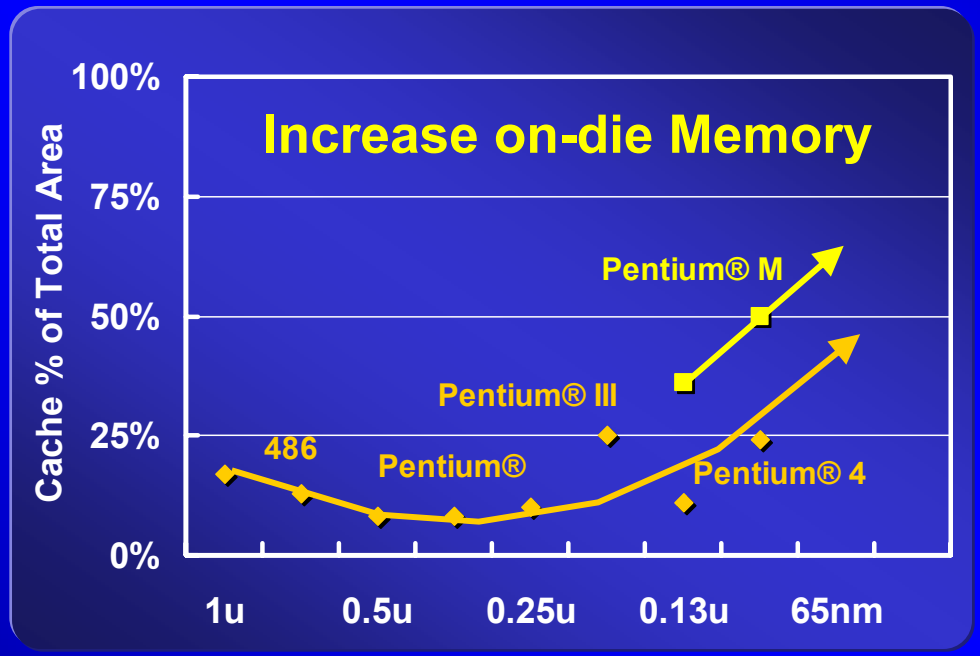
Pipeline Depth



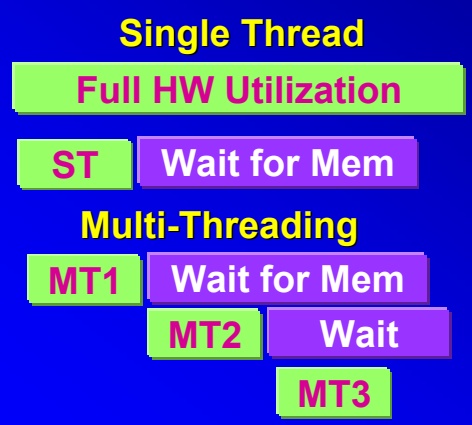
Pipeline & Performance

Maximum performance with
- **Optimum pipeline depth**
- **Optimum frequency**

μArchitecture Techniques

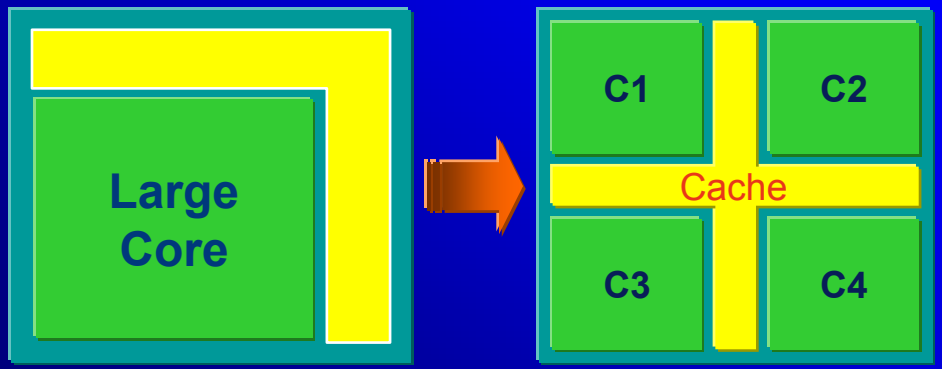


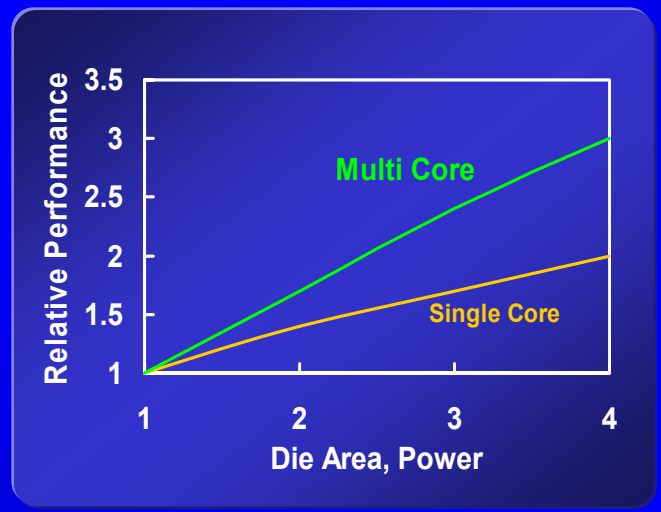
Multi-threading



Improved performance, no impact on thermals & power delivery

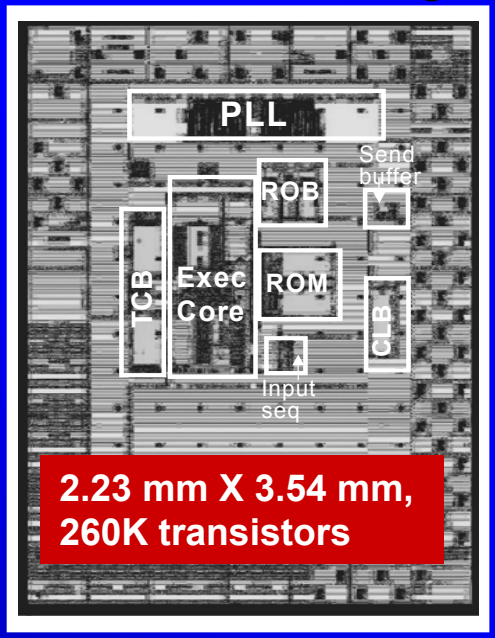
Chip Multi-processing

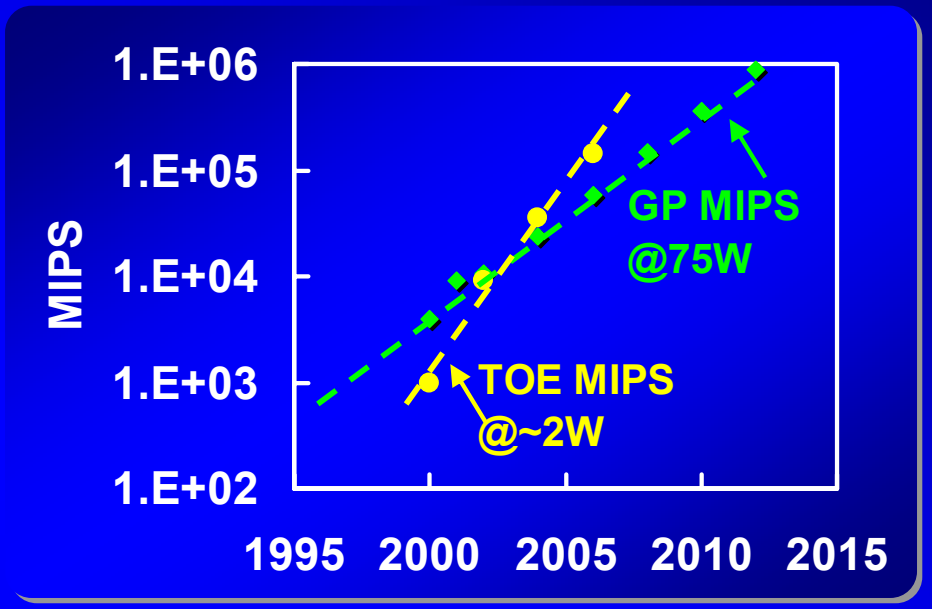




Special Purpose Hardware

TCP/IP Offload Engine

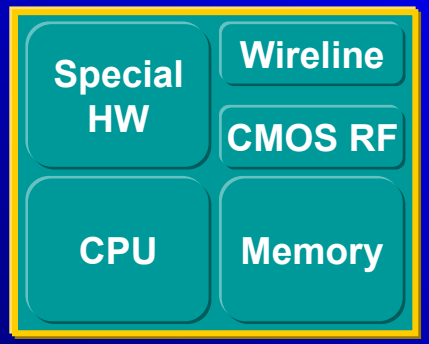




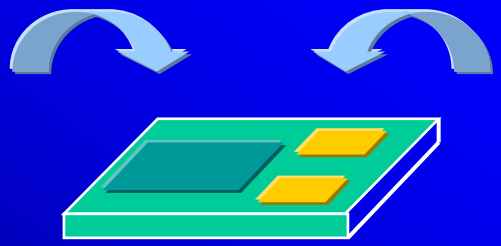
Opportunities: Network processing engines
MPEG Encode/Decode engines, Speech engines

Special purpose HW and extreme integration

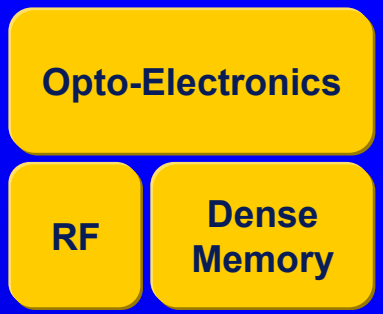
Si Monolithic



Polylithic

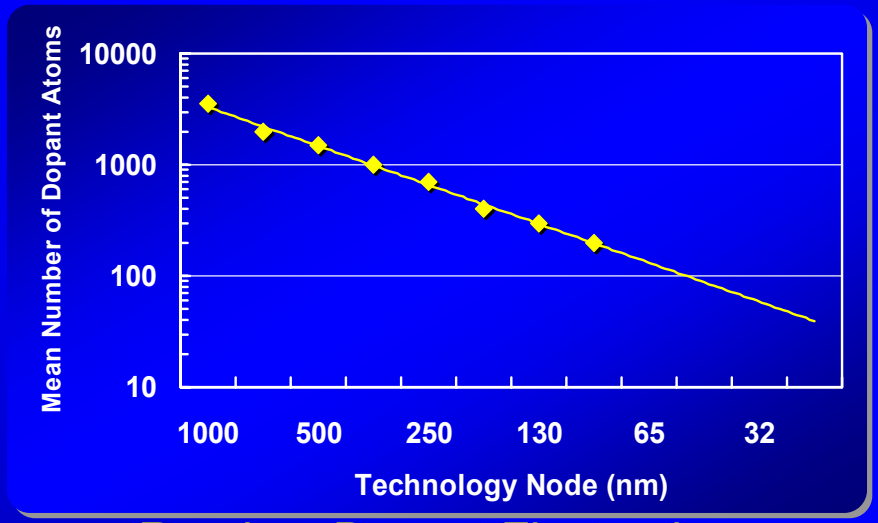


Heterogeneous
Si, SiGe, GaAs

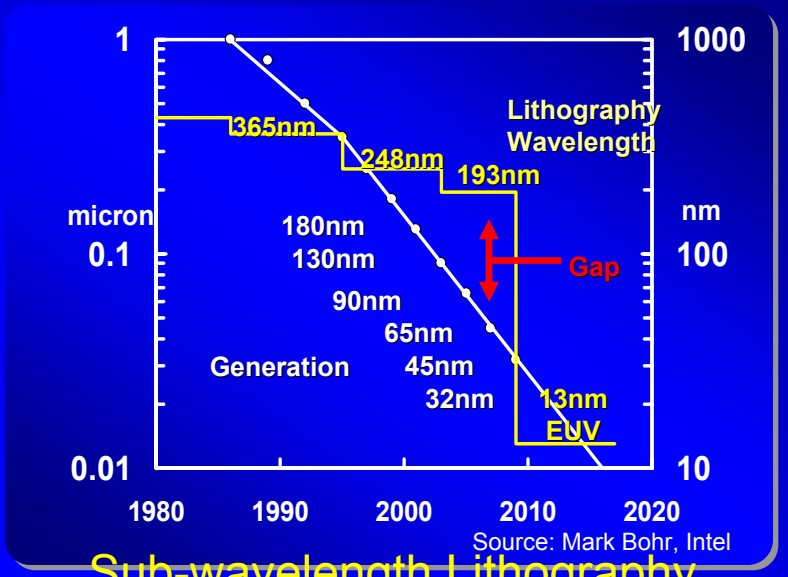



Variations

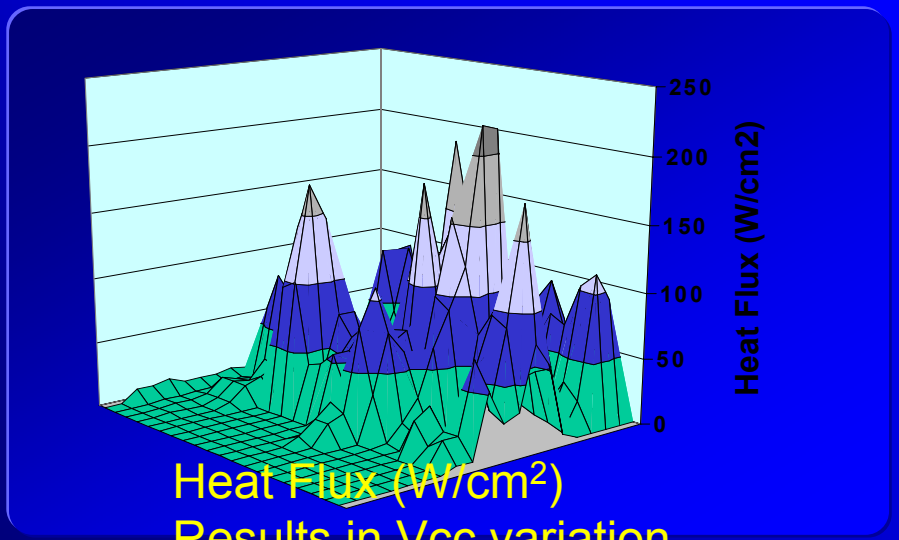
Sources of Variations



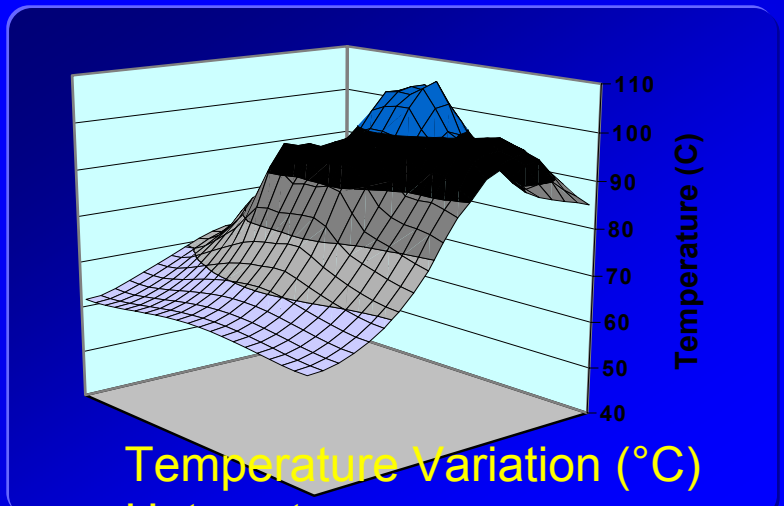
Random Dopant Fluctuations



Sub-wavelength Lithography



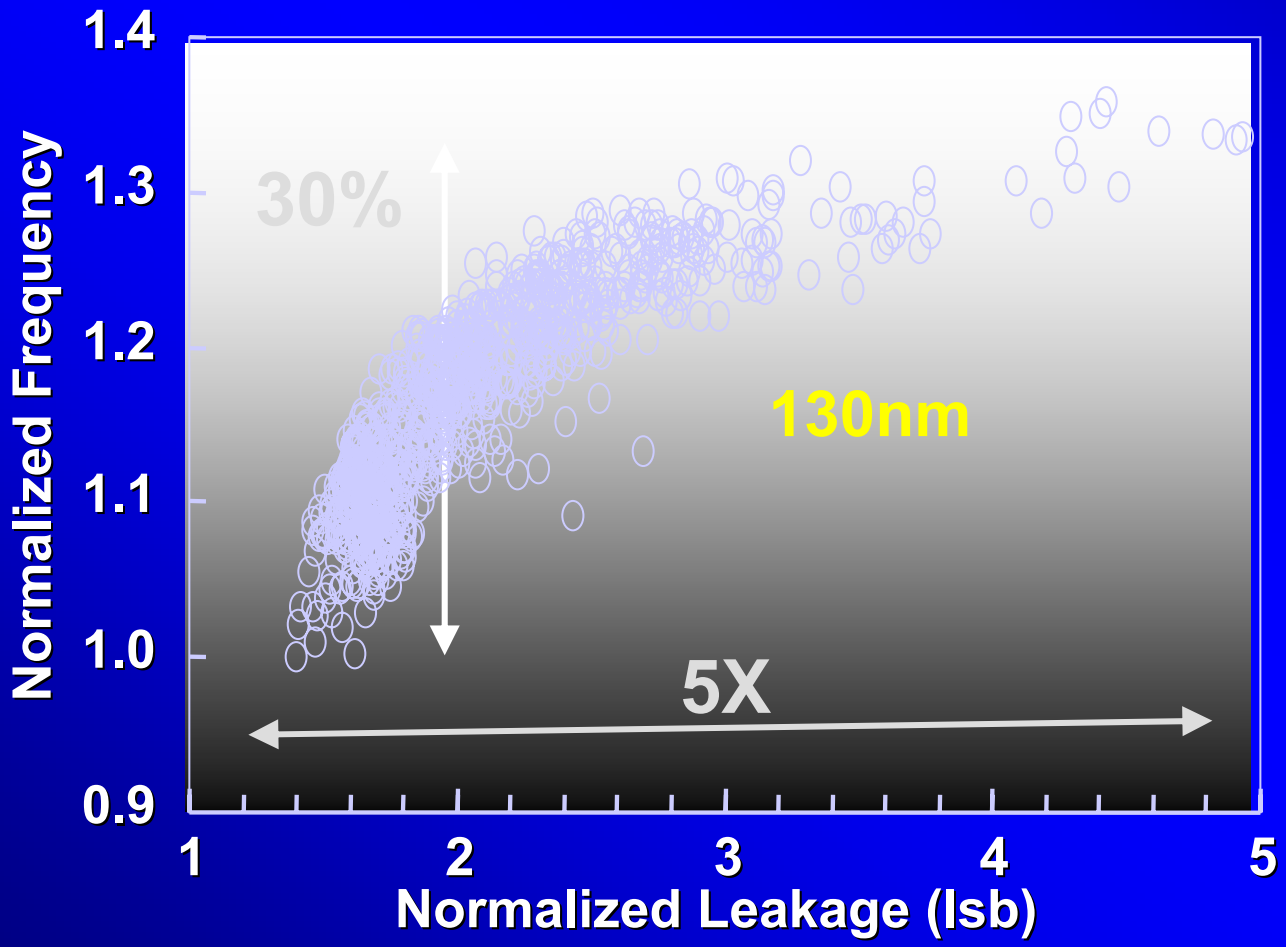
Heat Flux (W/cm^2)
Results in Vcc variation



Temperature Variation (°C)
Hot spots

Impact of Static Variations

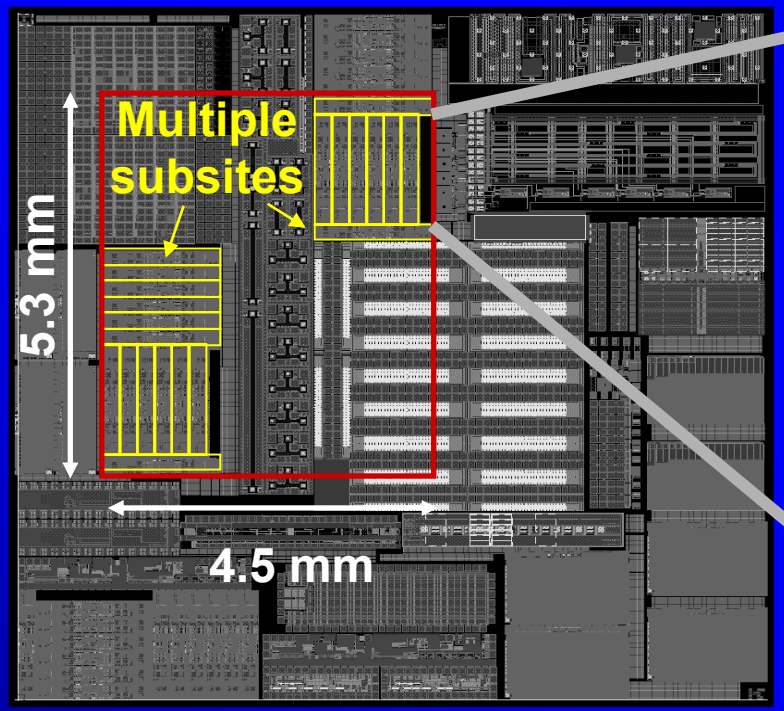
Today…

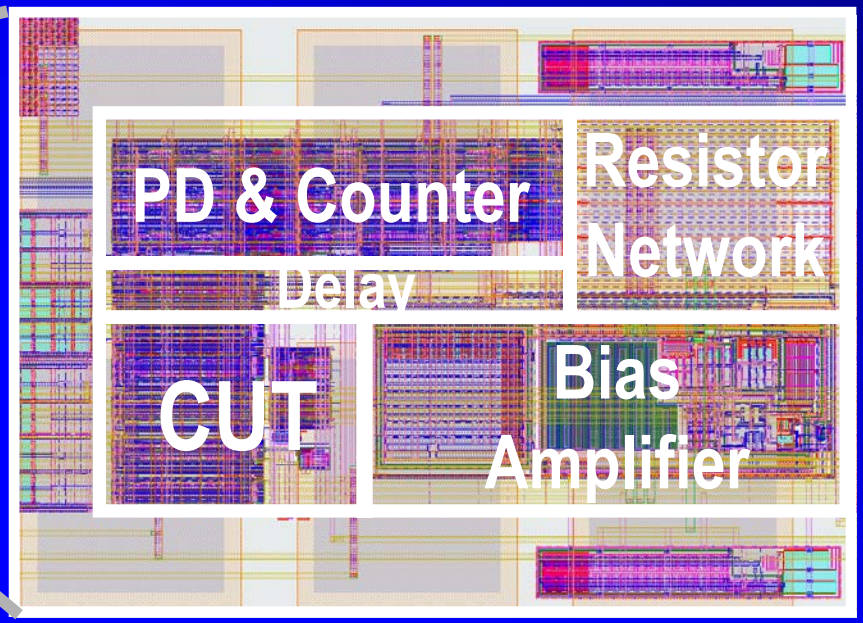


Frequency ~30%

Leakage Power ~5-10X

Adaptive Body Bias--Experiment





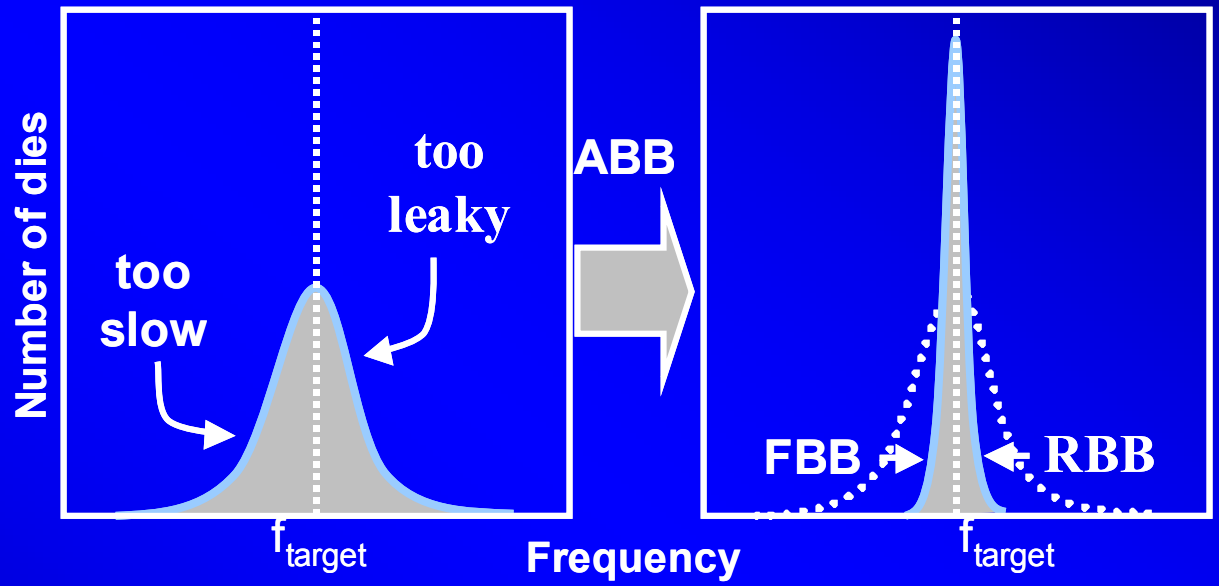
1.6 X 0.24 mm, 21 sites per die
150nm CMOS

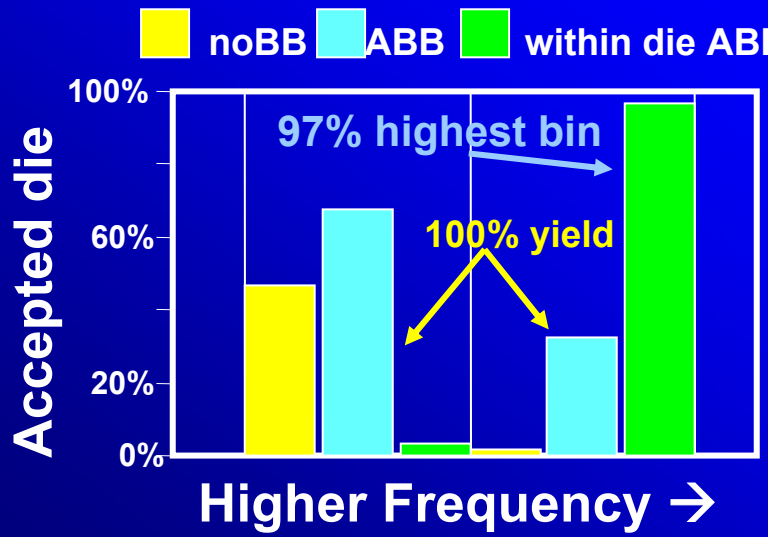
Technology	150nm CMOS
Number of subsites per die	21
Body bias range	0.5V FBB to 0.5V RBB
Bias resolution	32 mV

Die frequency: Min(F_1..F_{21})

Die power: Sum(P_1..P_{21})

Adaptive Body Bias--Results





For given Freq and Power density

- 100% yield with ABB
- 97% highest freq bin with ABB for within die variability

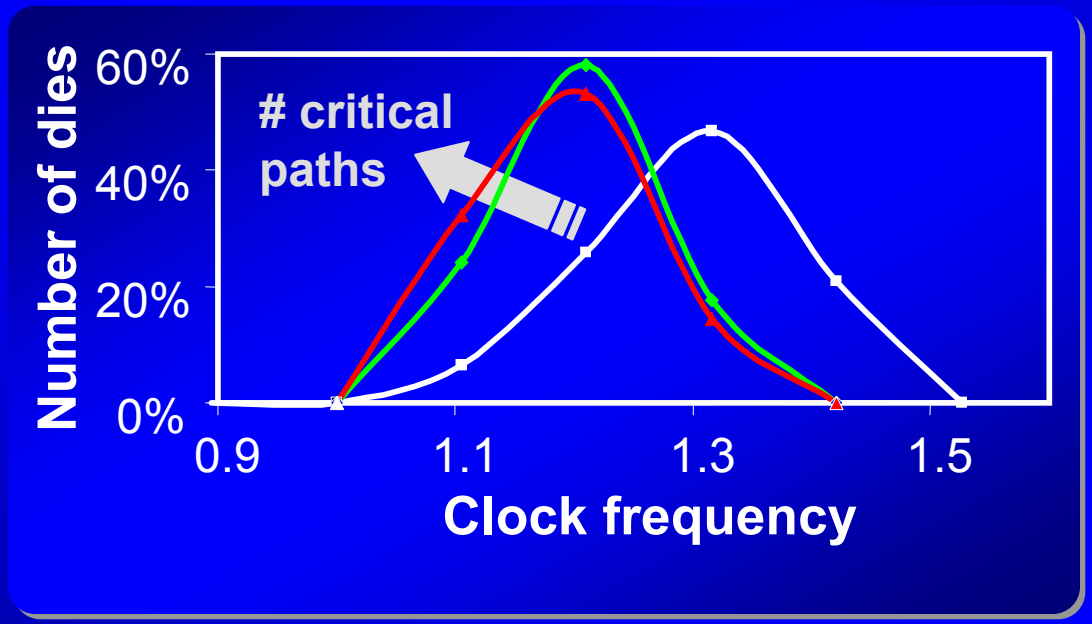
Circuit Design Tradeoffs

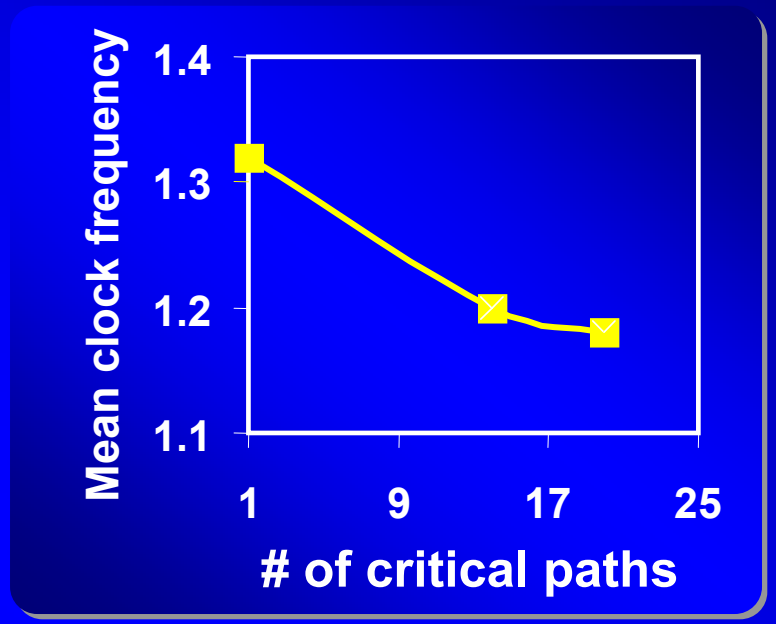
Higher probability of target frequency with:

1. Larger transistor sizes
2. Higher Low-Vt usage

But with power penalty

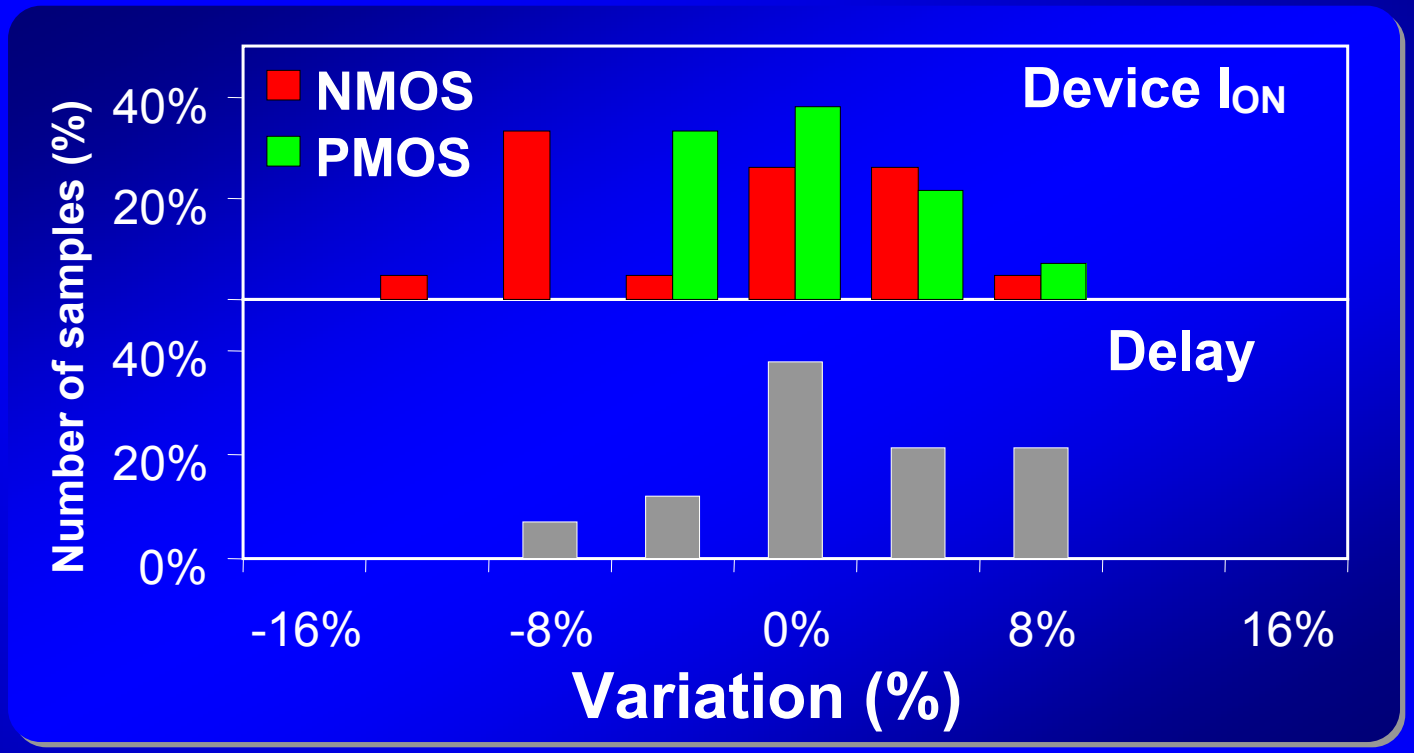
Impact of Critical Paths



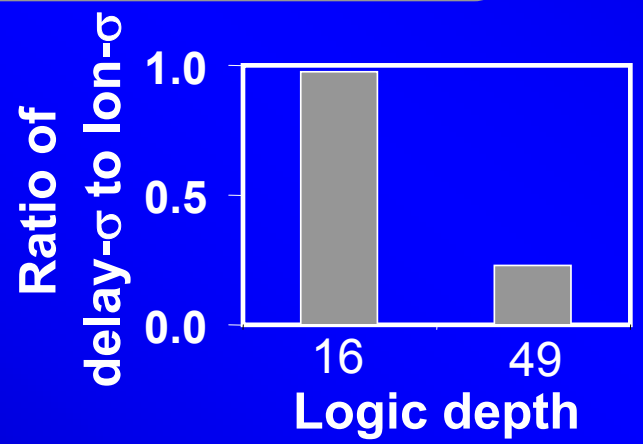


- With increasing # of critical paths
  - Both σ and μ become smaller
  - Lower mean frequency

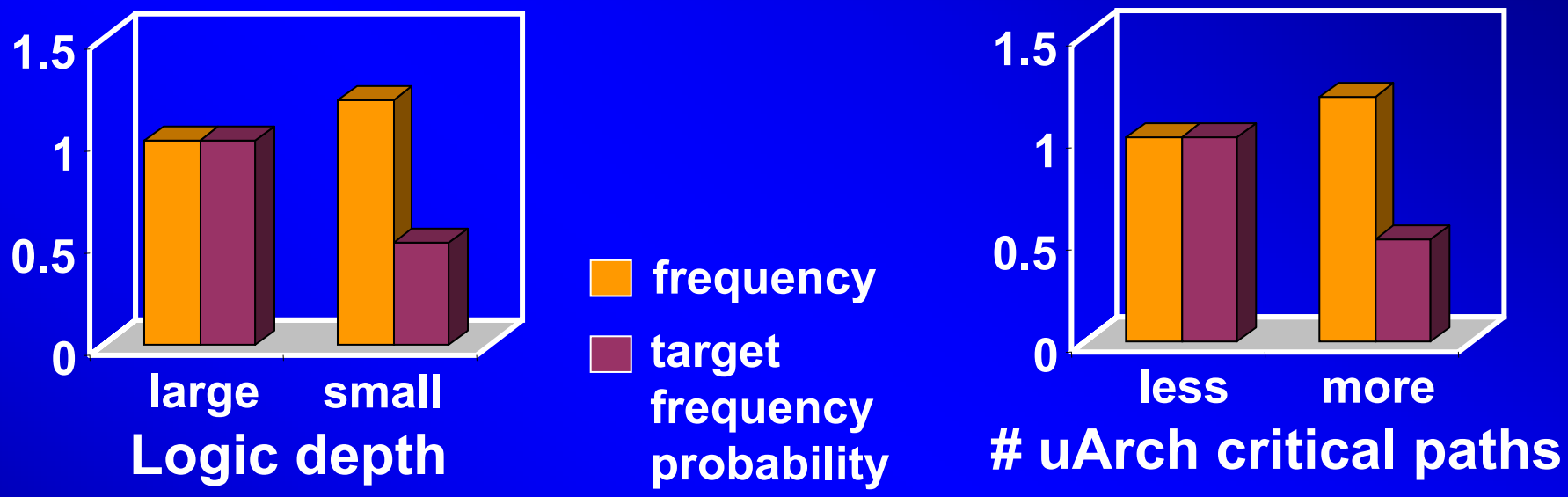
Impact of Logic Depth



Logic depth: 16		
NMOS Ion σ/μ	PMOS Ion σ/μ	Delay σ/μ
5.6%	3.0%	4.2%



μArchitecture Tradeoffs

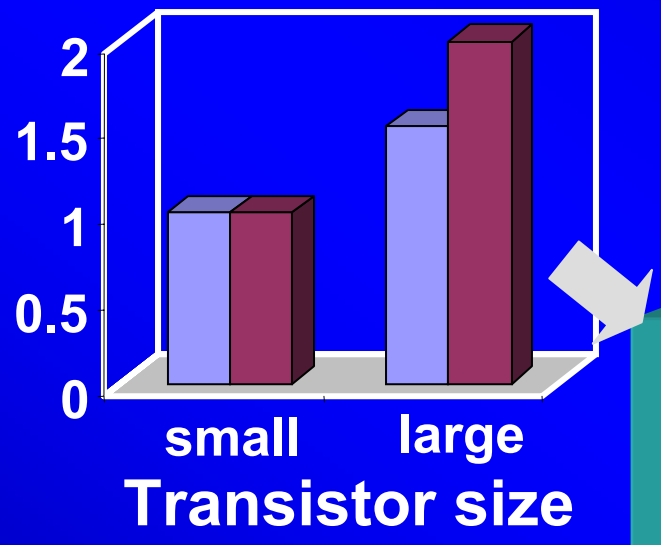


Higher target frequency with:

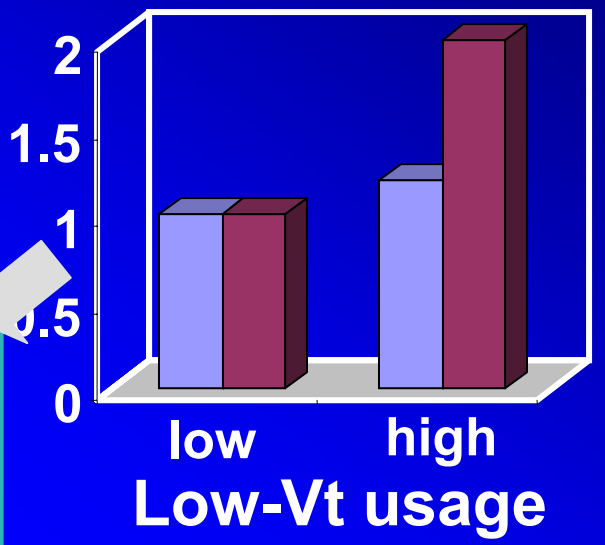
1. Shallow logic depth
2. Larger number of critical paths

But with lower probability

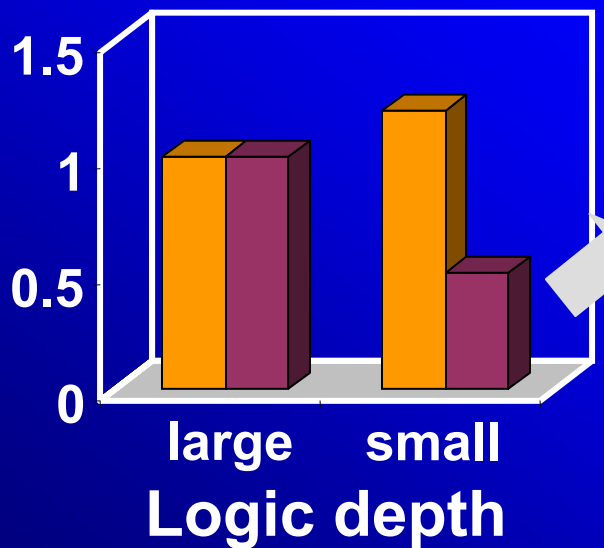
Variation-tolerant Design



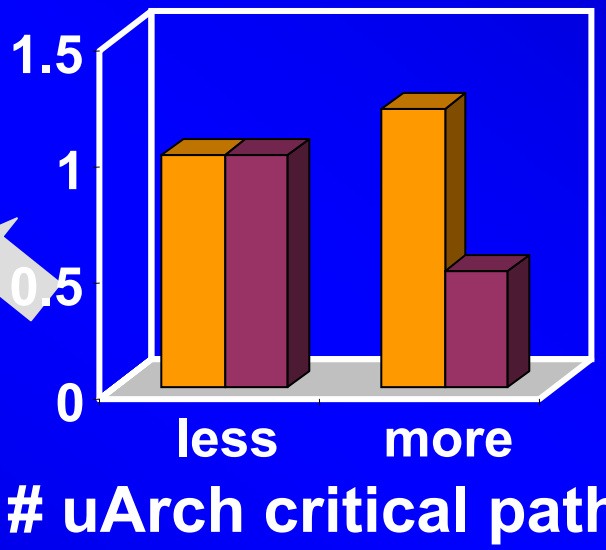
power
target frequency probability



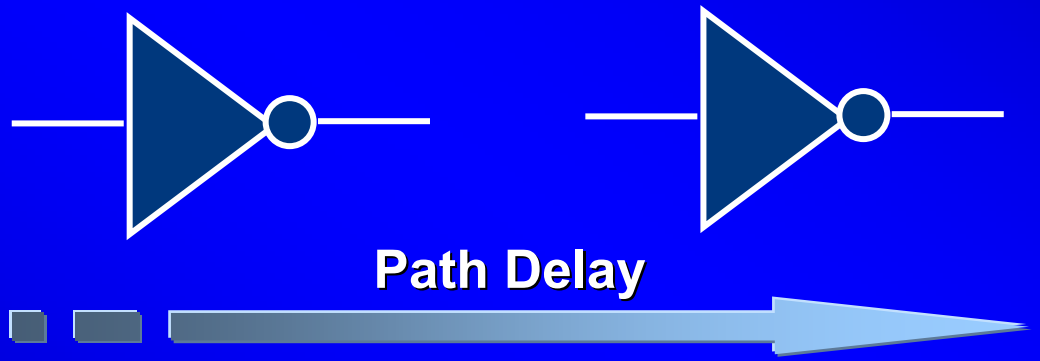
Balance power & frequency with variation tolerance

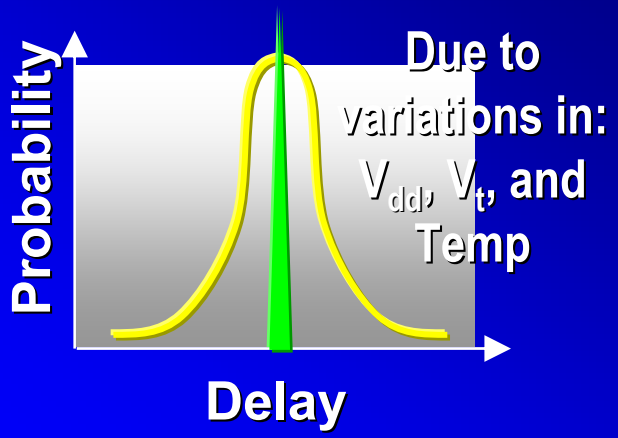


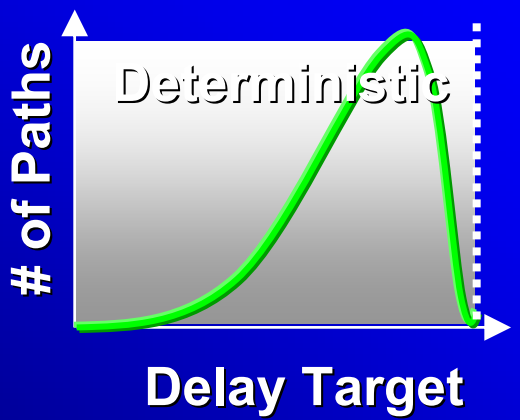
frequency
target frequency probability

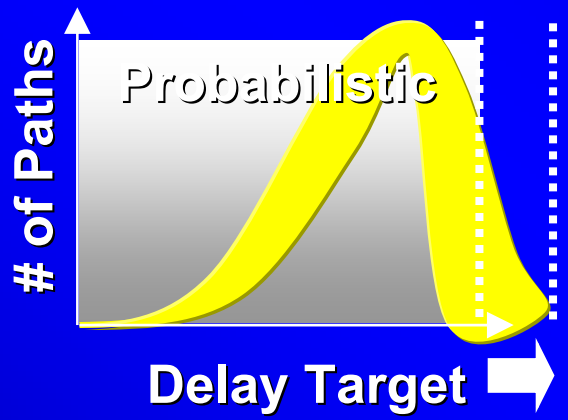


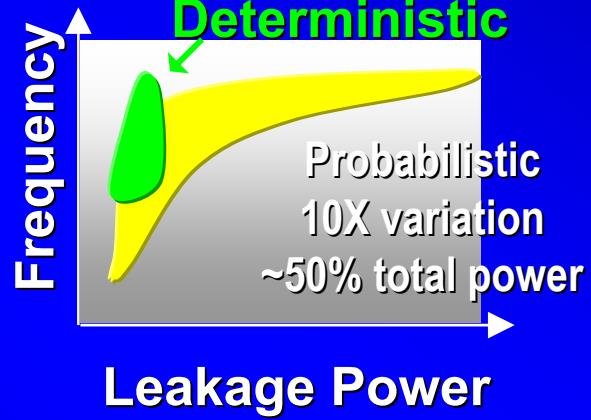
Probabilistic Design











Deterministic design techniques inadequate in the future

Shift in Design Paradigm

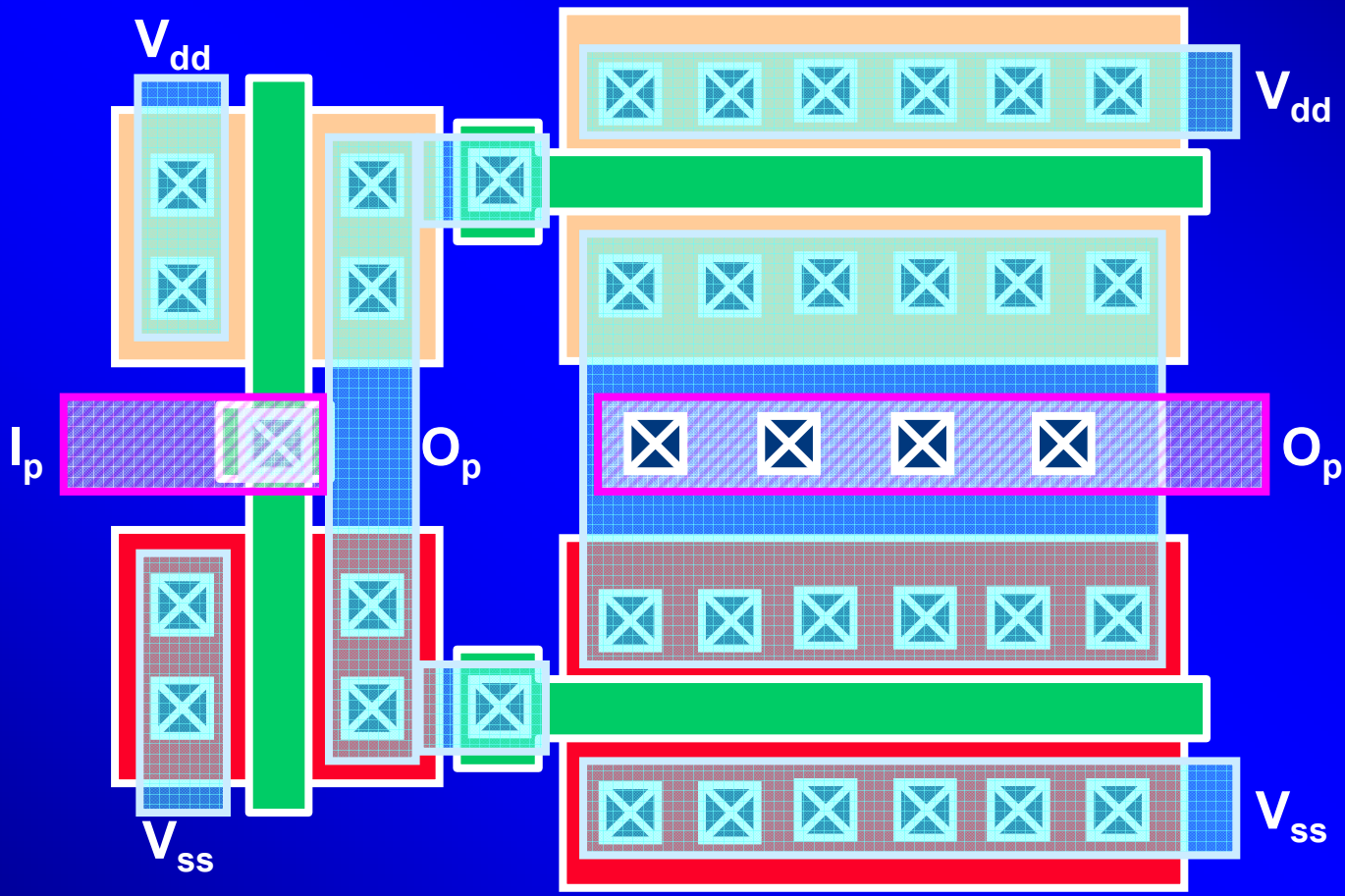
- Multi-variable design optimization for:
  - Yield and bin splits
  - Parameter variations
  - Active and leakage power
  - Performance

Today:
Local Optimization
Single Variable

Tomorrow:
Global Optimization
Multi-variate

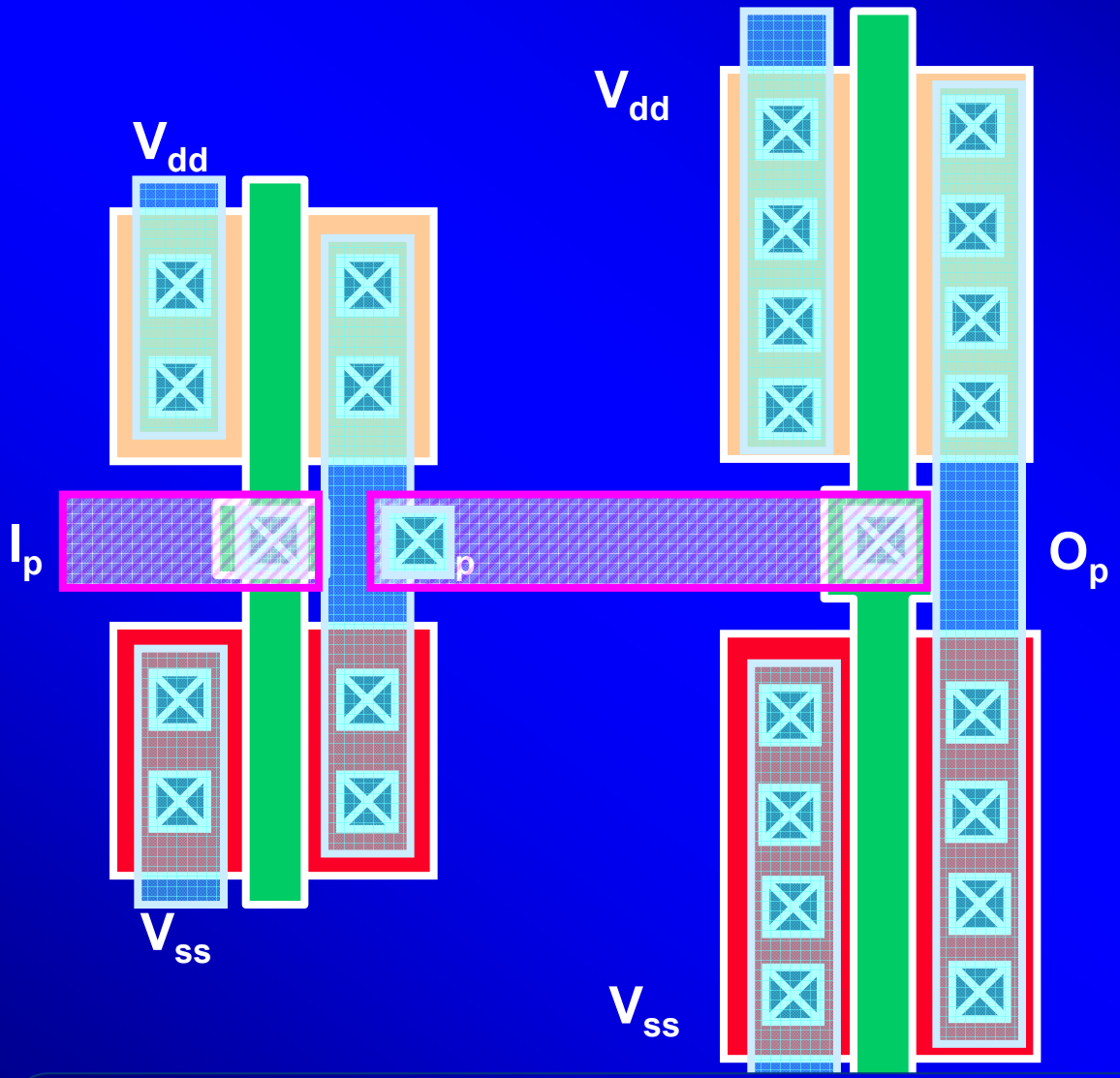
Physical design

Today's Freelance Layout



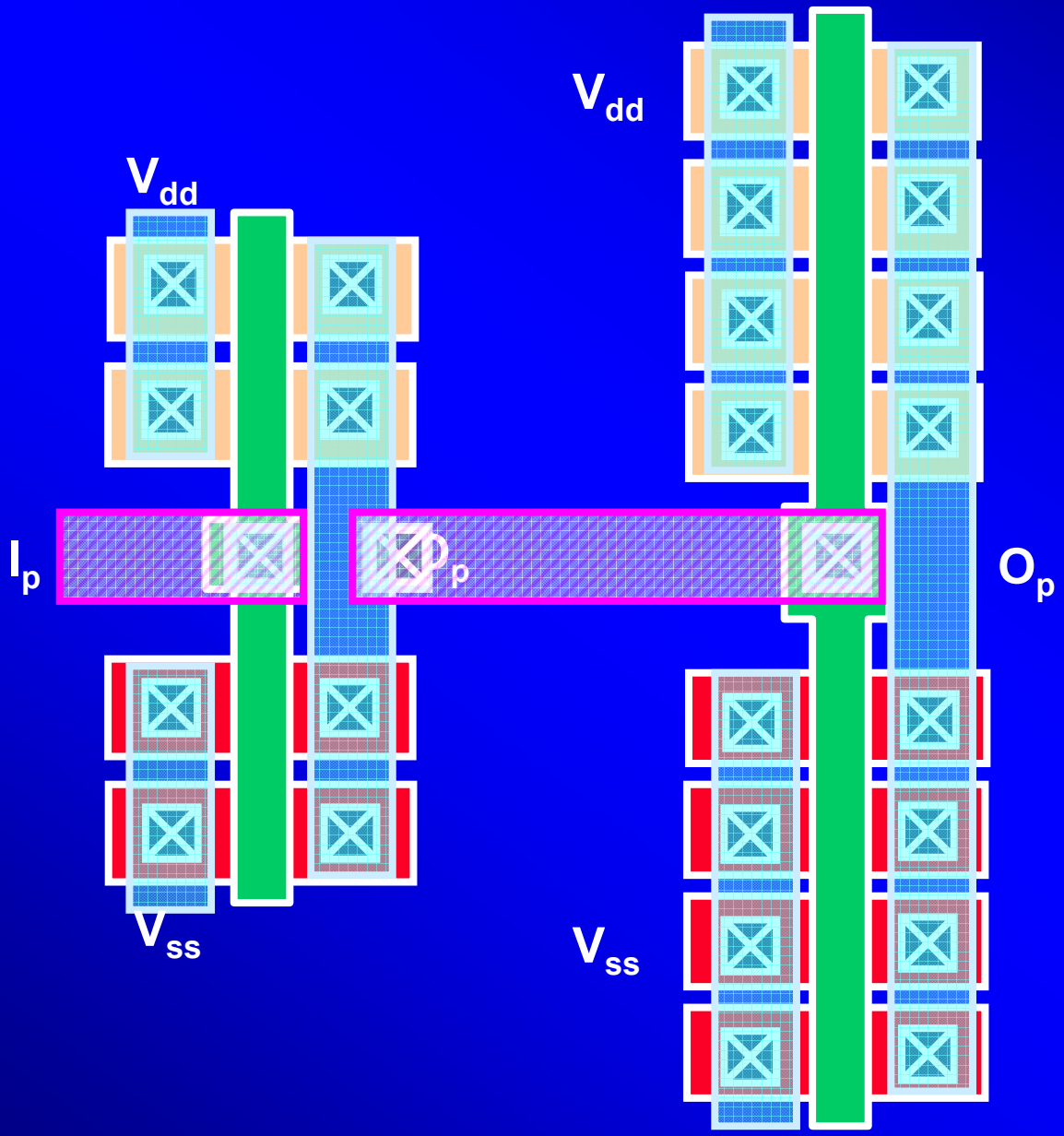
No layout restrictions

Transistor Orientation Restrictions

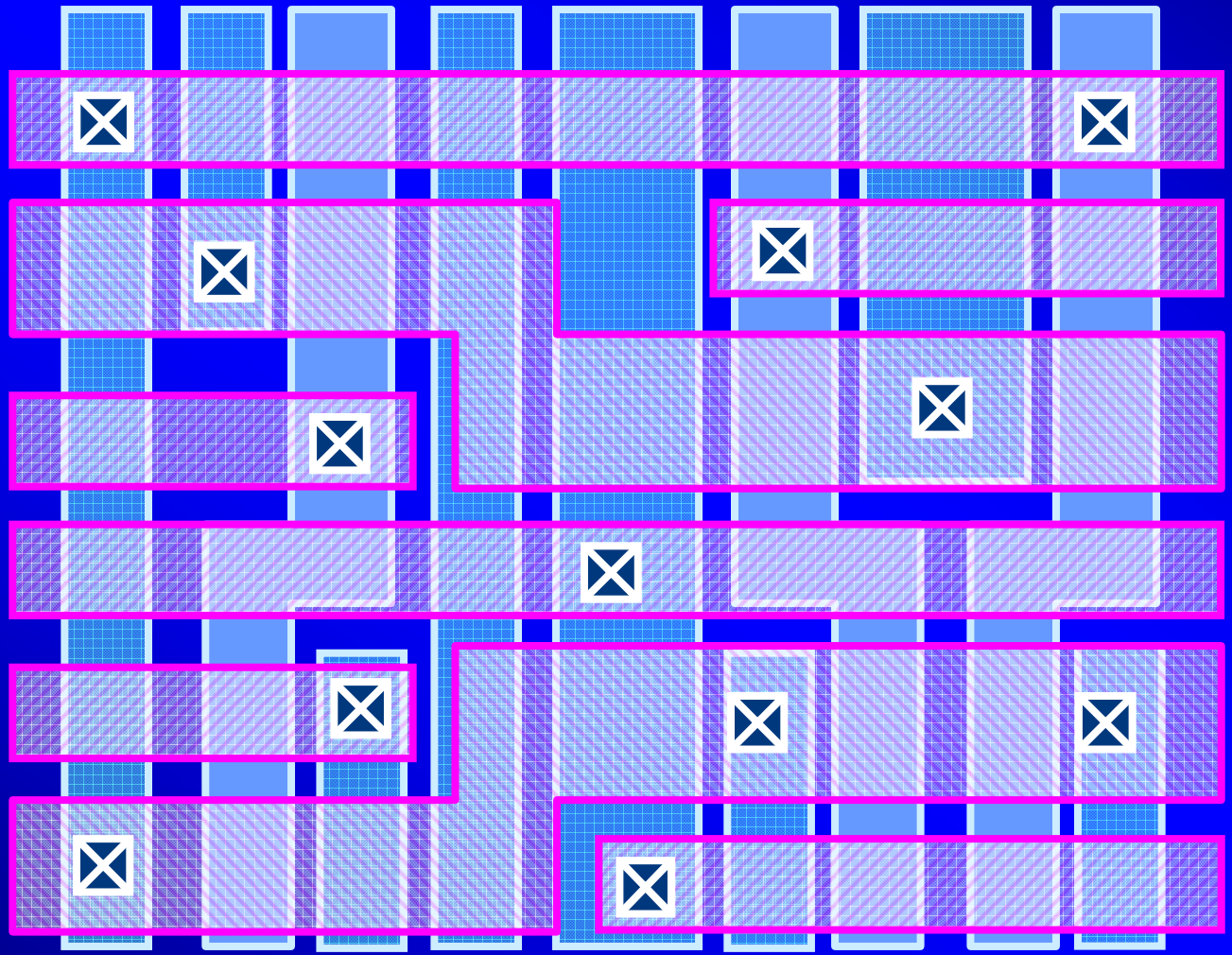


Transistor orientation restricted to improve manufacturing control

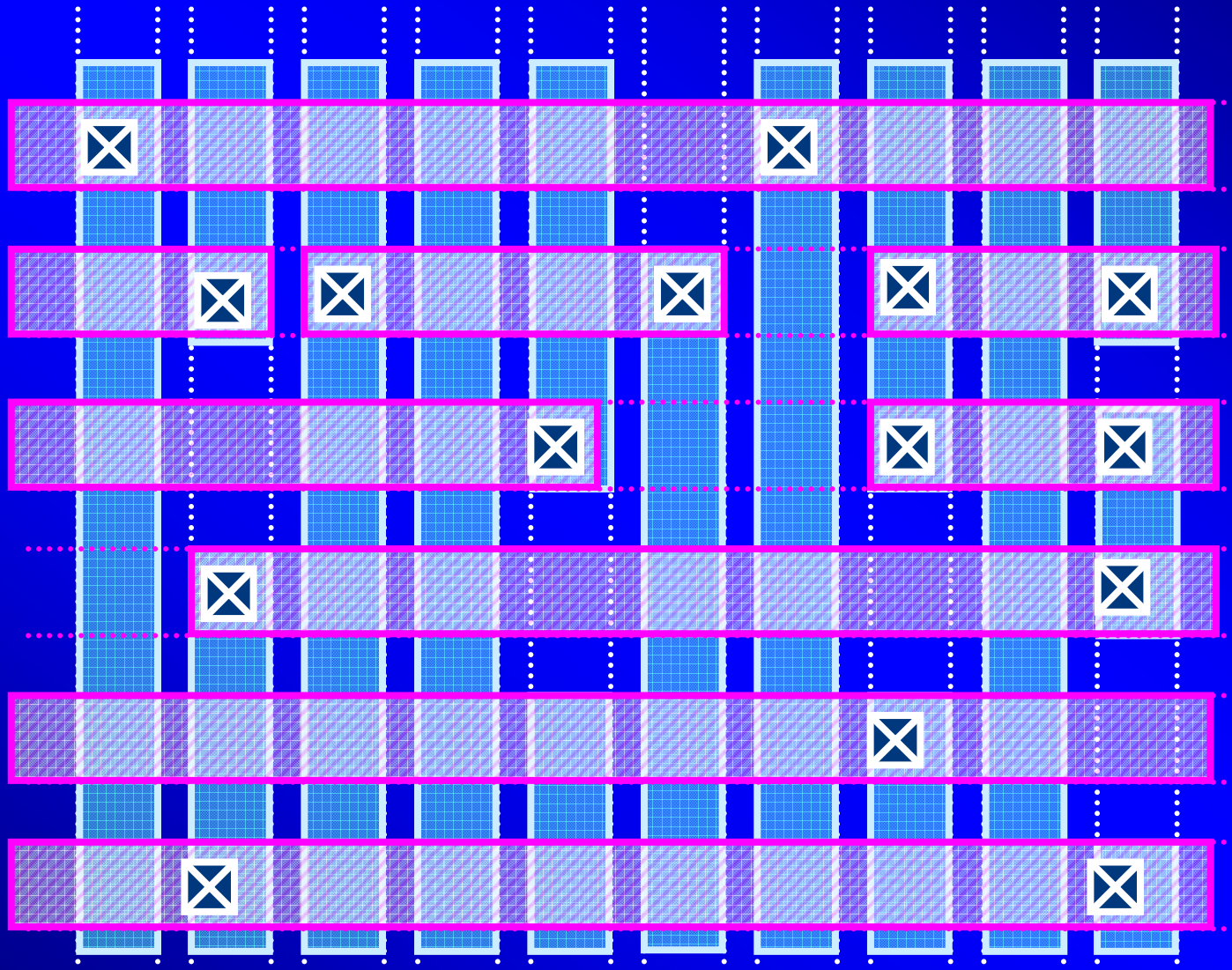
Transistor Width Quantization



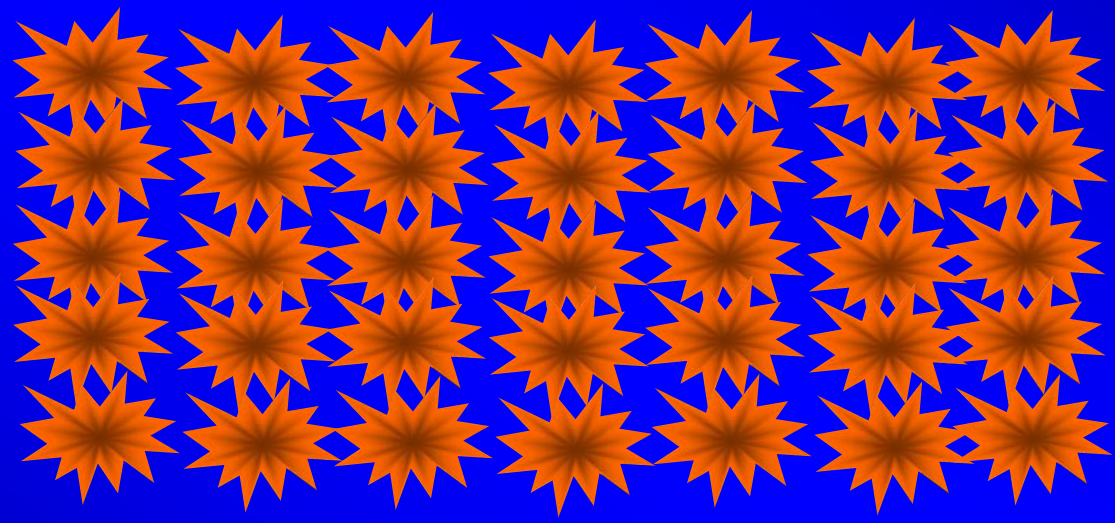
Today's Unrestricted Routing



Future Metal Restrictions

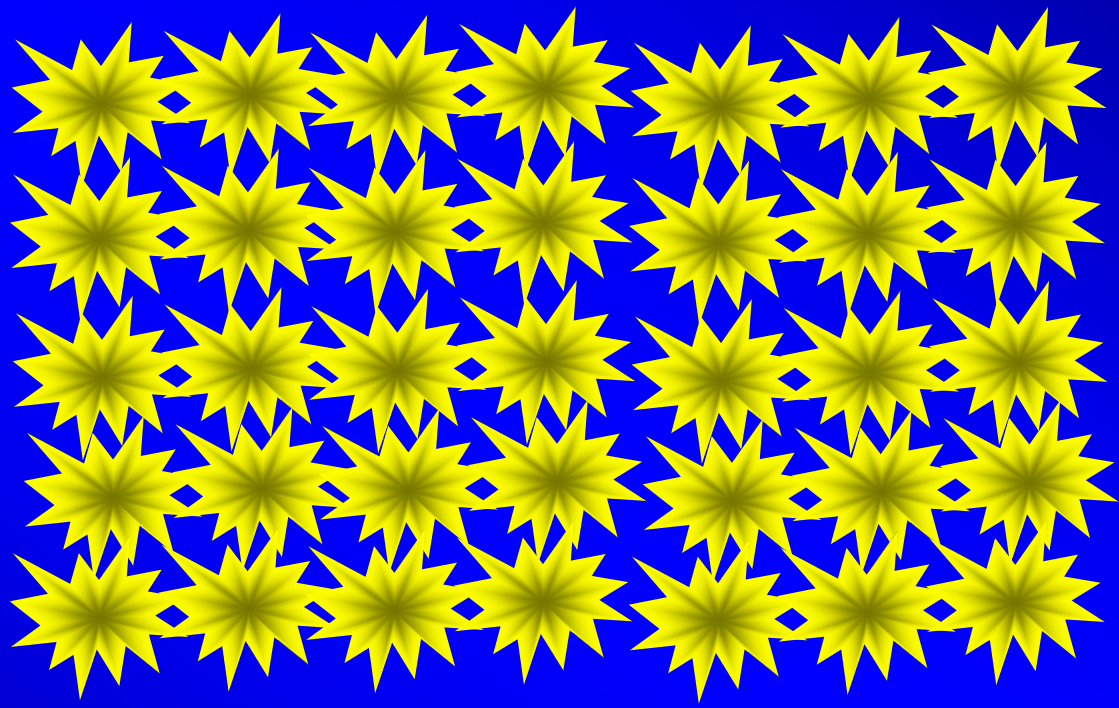


Today's Metric:
Maximizing Transistor Density



Dense layout causes hot-spots

Tomorrow's Metric:
Optimizing Transistor & Power Density



Balanced Design

Implications to Design

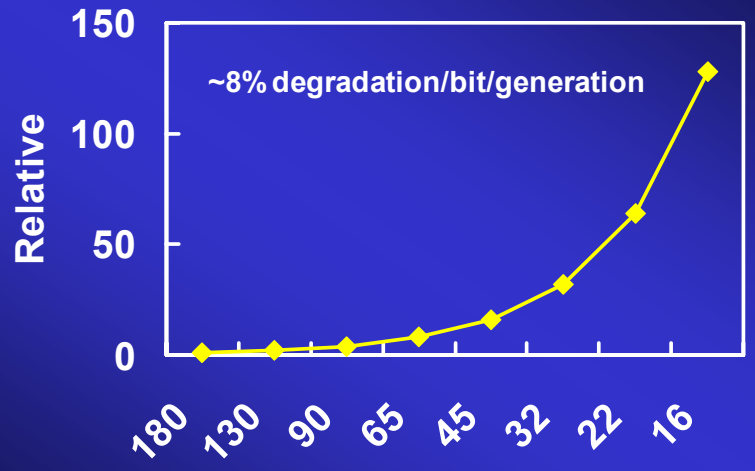
- Design fabric will be *Regular*
- Will look like *Sea-of-transistors* interconnected with regular interconnect fabric
- Shift in the design efficiency metric
  - From *Transistor Density* to *Balanced Design*

Extreme variations

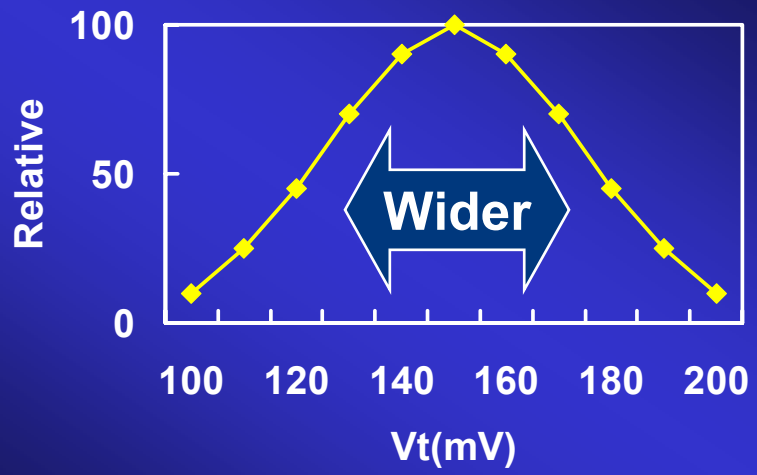
Technology Outlook

High Volume Manufacturing	2004	2006	2008	2010
Technology Node (nm)	90	65	45	32
Integration Capacity (BT)	2	4	8	16
Delay = CV/I scaling	0.7	~0.7	>0.7	Dela
Energy/Logic Op scaling	>0.35	>0.5	>0.5	Ener
Bulk Planar CMOS	High Probability			
Alternate, 3G etc	Low Probability			
Variability	Medium			Hig
ILD (K)	~3	<3		Redu
RC Delay	1	1	1	1
Metal Layers	6-7	7-8	8-9	0.5

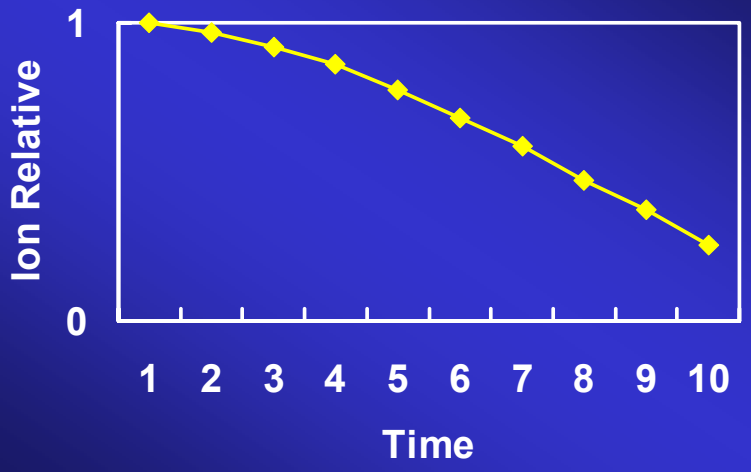
Reliability



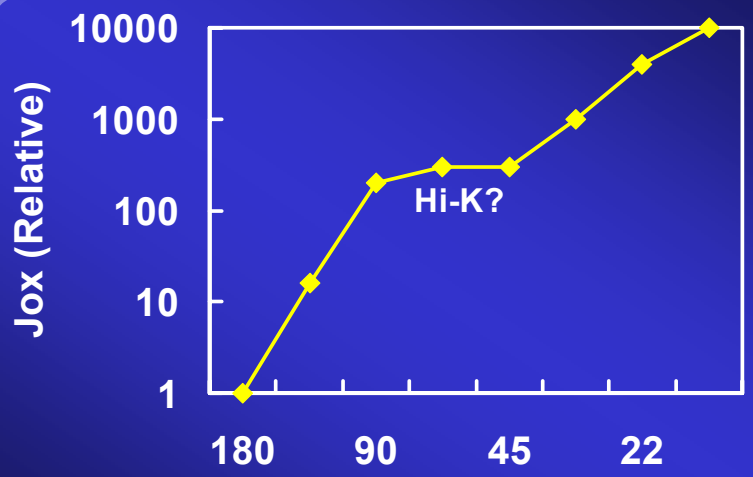
Soft Error FIT/Chip (Logic & Mem)



Extreme device variations



Time dependent device degradation



Burn-in may phase out…?

Implications to Reliability

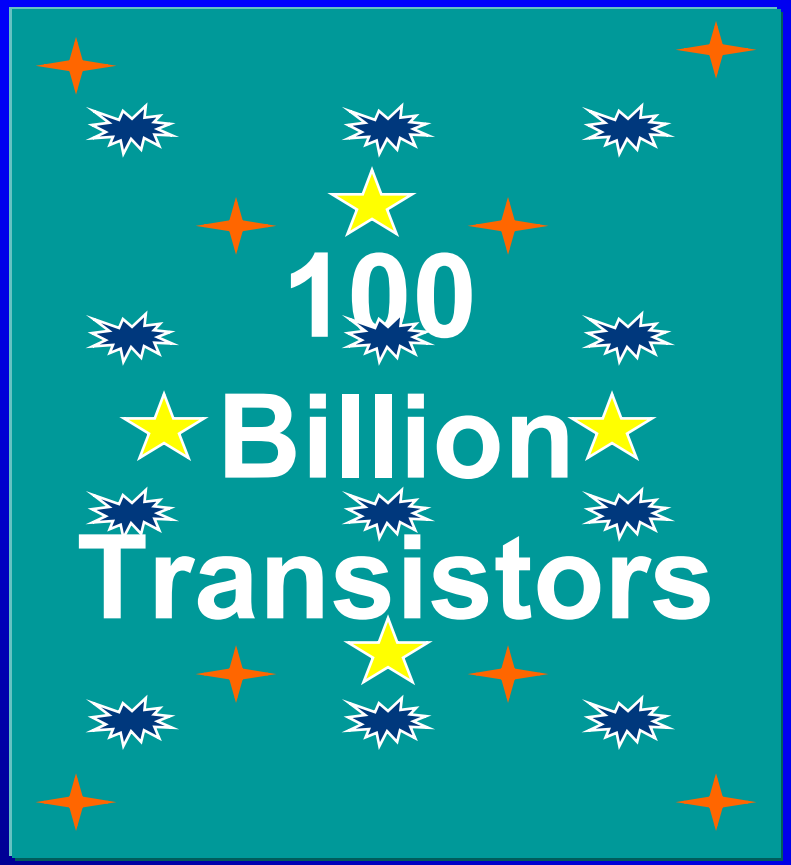
- Extreme variations (Static & Dynamic) will result in unreliable components
- Impossible to design reliable system as we know today
  - Transient errors (Soft Errors)
  - Gradual errors (Variations)
  - Time dependent (Degradation)

Reliable systems with unreliable components —Resilient μArchitectures

Implications to Test

- One-time-factory testing will be out
- Burn-in to catch chip infant-mortality will not be practical
- Test HW will be part of the design
- Dynamically self-test, detect errors, reconfigure, & adapt

In a Nut-shell…



100 BT integration capacity

20 BT unusable (variations)

10 BT will fail over time

Intermittent failures

Yet, deliver high performance in the power & cost envelope

Summary (of Challenges)

- Near term:
  - Optimum frequency & μArchitecture
  - Lots of memory & Multi—everywhere
  - Valued performance with higher integration
- Paradigm shift:
  - From deterministic to probabilistic design, with multi-variate optimization
  - Evolution of regular design fabric
- Long term:
  - Reliable systems with unreliable components
  - Dynamic self-test, detect, reconfigure, & adapt