Single-Chip Multiprocessors: The Next Wave of Computer Architecture Innovation

Guri Sohi
Computer Sciences Department
University of Wisconsin-Madison

Abstract

The past 25 years have been a very exciting time for computer architecture. A lot of this excitement was due to new opportunities made available by semiconductor technology: once basic uniprocessor functionality could be implemented on a chip, additional transistor resources could be used for innovative uniprocessor microarchitectures. The net result is that the microarchitecture of a high-performance uniprocessor today barely resembles that of one from 20 years ago. Today we stand at the doorstep of a similar period of excitement for multiprocessors. Semiconductor technology currently allows us to build a small chip multiprocessor. While the microarchitecture of the initial chip multiprocessors differs little from that of a traditional multiprocessor built with multiple chips, advances in semiconductor technology will allow us to rethink the microarchitecture of multiprocessors. Now is the time to start investigating innovative ways of architecting chip multiprocessors. This talk will try to provide some initial directions towards this overall research agenda.

Guri Sohi received a Ph.D. in Electrical and Computer Engineering from the University of Illinois in 1985. He has been a faculty member at the University of Wisconsin-Madison since graduation, and is currently the Chair of the Computer Sciences Department. Sohi's research has been in the design of high-performance computer systems. Topics that he has investigated in the past or continues to investigate include include dynamically scheduled instruction-level parallel processors, out-of-order execution with precise exceptions, non-blocking caches, decentralized microarchitectures, speculative multithreading, computation reuse, memory dependence speculation and prediction, value degree of use prediction, and chip multiprocessors.

He received the 1999 ACM SIGARCH Maurice Wilkes award "for seminal contributions in the areas of high issue rate processors and instruction level parallelism." At the University of Wisconsin he was selected as a Vilas Associate in 1997 and won the WARF Kellett Mid-Career Faculty Researcher award in 2000.