Making the Right Hand Turn to Power Efficient Computing

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Outline

- Technology scaling
- Types of efficiency
- Making the right hand turn
Historic Perspective

- **Size**
  - V Tubes
  - Bipolar
  - NMOS
  - CMOS

- **Gate Delay**
  - V Tubes
  - Bipolar
  - NMOS
  - CMOS

- **Energy/Transition**
  - V Tubes
  - Bipolar
  - NMOS
  - CMOS

Scaling will continue

V Tubes $\Rightarrow$ Bipolar
Bipolar $\Rightarrow$ NMOS
NMOS $\Rightarrow$ CMOS
CMOS $\Rightarrow$ ?
Technology scaling is a great thing.

<table>
<thead>
<tr>
<th>X &amp; Y Dimensions scale down by 30%</th>
<th>Doubles transistor density</th>
</tr>
</thead>
<tbody>
<tr>
<td>Z-Oxide thickness scales down</td>
<td>Faster transistor, higher performance</td>
</tr>
<tr>
<td>Vcc &amp; Vt scaling</td>
<td>Lower active power</td>
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Supply Voltage Scaling

Supply voltage scaling has slowed.
Active Power Projection

Power will limit transistor integration

Assumptions:
- 15% Vdd scaling
- 50% Freq scaling (Per generation)
Sub-threshold Leakage

MOS Transistor Characteristics

Transistors will be *dimmers*, not *switches*
Excessive sub-threshold leakage power

Assumptions:
- 15% Vdd scaling
- 5X Ioff scaling
(Per generation)
**Variations in P, V, and T**

- **Process**
  - Die-to-die variation
  - Within-die variation
  - Static for each die

- **Voltage**
  - Chip activity change
  - Current delivery RLC
  - Dynamic: ns to 10-100us
  - Within-die variation

- **Temperature**
  - Activity & ambient change
  - Dynamic: 100-1000us
  - Within-die variation
Impact of Critical Paths

Impact of transistor parameter variations:
- Wide distribution of circuit frequency
- Lower mean freq with # of critical paths
- Encourages more localized, clustered designs
Tough Platform Demands

- Shrinking volume
- Reduced Noise
- Yet, Higher Performance

At Odds

- Reduced thermal budget
- Higher heat sink volume
- Higher air flow rate
**BOM Cost Squeeze**

![Graph showing desktop PC ASP with Performance and Value axes.](graphic)

- **Source:** Dataquest Personal Computers

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**Budget for power and cooling is shrinking**

- **$2000 PC cost ('97)**

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**Desktop PC ASP**

- **1995:** $2200
- **1996:** $1800
- **1997:** $1500
- **1998:** $1400
- **1999:** $1300
- **2000:** $1200

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**Source:** Dataquest Personal Computers
Data Centers: Rack Mount Limits

Wasted space and higher cost in future

Power (Watts)

2002  2006

Network Equipment (~28%)
Servers & Storage (~15%)
Data Center Cooling Capability (~8%)
75-100 W/sq. ft
150-200 W/sq. ft

Rack Utilization

4X Cost
Outline

- Technology scaling
- Looking at efficiency
- Making a right hand turn
Power Efficiency

In the same process technology, compare:
- Scalar ⇒ Super-scalar
- Dynamic
- Deep pipe

2-3X Growth in area
~1.4X Growth in Integer Performance
~1.7X Growth in Total Performance
2-2.5X Growth in Power

2-2.5x growth in power / generation
Energy Efficiency

20-30% drop in energy efficiency / generation
Circuit Efficiency

Assumptions:
Activity: Static = 0.2,
Domino = 0.5
Clock consumes 40% of full chip power

Faster circuits contribute to power inefficiency.
Outline

• Technology scaling
• Types of efficiency
• Making a right hand turn
Power Comes First

Business as usual is not an option
Low Power and High Performance

- **Maximize battery life (fixed energy)**
  \[
  \text{Energy} = T_{\text{exec}} \times \text{Power} \approx (1/\text{Perf}) \times \text{Power}
  \]
  Increasing the Performance by 10% and the Power by 10% will end up with same battery life

- **Maximize performance within a given power envelope (Thermal constrains)**
  \[
  f \approx K \times V
  \]
  \[
  \text{Power} = \alpha \times C \times V^2 \times f \approx \alpha \times C \times f^3
  \]
  \[
  \Delta \text{Power}/\text{Power} = ((f+\Delta f)^3 - f^3)/f^3 \approx 3 \Delta f/f
  \]
  \[
  \text{Perf} = \text{IPC} \times f
  \]
  ➔ The right trade off between Performance and Power

\[\Delta \text{IPC} < 3 \Delta \text{Power is the metric}\]
“Less is More”

- Strive to accomplish the same task in less energy and less time
  - Higher performance at lower energy can always be traded with same performance at lower power

- Methodology works at all levels
  - Aggressive clock gating
  - Caching - dumb and smart
  - Better branch predictors
  - Smart work reduction
  - Prioritize useful over speculated work
  - Fixed functions
“Less is More” in Banias

- Improved branch prediction
  - Over 20% fewer branch mispredictions
- Dedicated stack manager
  - Over 5% uop reduction
- Uop fusion
  - Over 10% uop reduction
- Big L2 cache

Achieving Higher Performance at Lower Power
Reducing Active Power

Multiple Supply Voltages

Slow → Fast → Slow

Low Supply Voltage → High Supply Voltage

Throughput Oriented Design

Logic Block

Freq = 1
Vdd = 1
Throughput = 1

Logic Block

Freq = 0.5
Vdd = 0.5
Throughput = 1
Power = 0.25
Area = 2
Pwr Den = 0.125
Critical Scheduling

- Large schedule window (ILP)
- Exploit instruction criticality
  - Latency tolerant bypass
  - Limited critical resources

Data Mgmt System

Large Slow Schedule Window

Register File

Small Fast Schedule Window

Fast Cluster

Slow Cluster

50-60% non-critical

40-50% critical

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Recycling Waste

- Wasted execution
  - Spec Exec vs Retired
  - ~30% in 1st gen OOO
  - ~60% in 2nd gen OOO
  - ~160% in future

- Leverage info from wasted execution

- Improve branch Prediction
  - 30% reduction in misprediction rate
  - 18% to 48% less wasted execution

- Can we reuse some of the execution result too?
Efficiency Through xMT

Thermals & power delivery designed for full HW utilization

Multithreading improves performance without impacting thermals & power delivery
**Power Efficient Asymmetric Threads**

- **Function Asymmetric Threading** (w/co-processor ISA)
  - Partition single thread into a main thread with special function threads
  - Special function unit is more area and power efficient

- **Performance Asymmetric Threading** (ISA compatible)
  - Serial code on heavy core
  - Parallel code on smaller and power efficient core
Chip Multi-Processing

- Multi-core, each core MT
- Shared cache and front side bus
- Each core has different Vdd & Freq
- Core re-cycling to spread hot spots
- Lower junction temperature
Summary

• Technology scaling can and will continue

• Challenges to power and energy efficiency are real but surmountable..

• ..through evolutionary approaches to circuits and microarchitecture