Linearizing Irregular Memory Accesses for Improved Correlated Prefetching

Akanksha Jain, Calvin Lin

The Problem

Prefetch irregular but correlated memory accesses

Address Correlation: A, X, C, E, D, Y, B form a temporally correlated stream

PC-Localization: Segregate the global stream by the load instruction’s PC to improve predictability
- A, C, E, D, B is one PC-localized stream
- X, Y is another PC-localized stream

ISB is the first prefetcher to combine Address Correlation and PC-Localization (PC/AC)

Our Solution

Replace the GHB with a new organization

Physical Address Space

Indirection

Structural Address Space

Regular Prefetching

Layer of indirection
- Map PC-Localized correlated addresses to consecutive addresses in the structural address space

Three benefits:
1. Combines address correlation and PC-localization
2. Novel meta-data caching scheme that synchronizes on-chip meta-data with the TLB
3. Trains on the LLC access stream

Comparison with the GHB

1. For address correlation, GHB is located off-chip
2. PC-localization requires a linked list traversal

Limitations of the GHB:
1. Combining address correlation and PC-localization is prohibitively expensive
2. Temporal organization makes caching difficult
3. Trains on the miss stream to reduce off-chip accesses

Evaluation

Comparison of irregular prefetchers (degree 1)

Impact of prefetch degree on accuracy

Performance

<table>
<thead>
<tr>
<th></th>
<th>STMS [Wenisch 09]</th>
<th>Our Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speedup</td>
<td>8.3%</td>
<td>23.1%</td>
</tr>
<tr>
<td>Accuracy</td>
<td>58.6%</td>
<td>93.7%</td>
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</table>

Cost

<table>
<thead>
<tr>
<th></th>
<th>STMS [Wenisch 09]</th>
<th>Our Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traffic Overhead</td>
<td>~ 35%</td>
<td>8.4%</td>
</tr>
<tr>
<td>On-chip Budget</td>
<td>10KB</td>
<td>8KB – 32KB</td>
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