Warped-GATES
Gating Aware Scheduling and Power Gating for GPGPUs

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Power Gating Challenges in GPUs

- Scheduler greedily issues ready instructions
  - Agnostic to instruction type.

Scheduler

<table>
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<tr>
<th>INT</th>
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<th>FP</th>
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Diagram:

- Scheduler
- INT, INT, INT, INT
- FP, FP, FP, FP
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Proposed Techniques

- **Gating Aware Scheduler (GATES)**
  - Gives priority to same instruction type during scheduling.
  - Is able to increase the length of the idle periods.
  - **Idle periods are not long enough to avoid negative savings!!**

- **Blackout technique**
  - Eliminates negative savings by forcing the unit to stay in power gating state.

\[
\begin{align*}
1.5X & \quad \text{Static Power Savings} \\
<1\% & \quad \text{Performance Overhead}
\end{align*}
\]