Transactional Memory Architecture and Implementation for IBM System z

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Transactional Memory in System z

- Transactional Execution introduced in latest mainframe generation: zEC12
- First commercially available TM implementation in general-purpose CPU
- Available since September 2012

- zEC12 is descendent of original System 360 mainframe from 1964
- System z design is focused on
  - performance
    - 5.5GHz, out-of-order 6-way superscalar CISC processor
  - scalability
    - 101 customer CPUs, rich SMP-fabric, and large caches
  - availability
    - 99.999% availability, through stack-optimization for RAS
  - virtualization
    - up to 60 partitions and thousands of virtual images

- targeting mission critical computing for commercial workload
  - Transactional & analytical database workloads
  - SAP, Java, Websphere, …
- IBM System z is IT backbone of many of the worlds largest corporations
Transactional Execution
Requirements for introduction into commercial computer system

- **Ease of use → simple semantics**
  - System z has “strong memory ordering” architecture, easing parallel software design
  - Limit exposure of micro-architectural behavior at architecture level

- **Stepwise introduction into existing software**
  - Millions of lines of code won’t be rewritten in a year
  - Transactions need to co-exist with lock-based serialization

- **Future compatibility**
  - Software cannot be adjusted for every generation of hardware

- **Debugging & RAS**
  - Parallel programming is hard – cannot make it harder with debugging and reproducibility problems

- **Introduction into existing CPU & Cache base design**
  - CPU & SMP-fabric evolutionary designs, revolutions are too expensive & risky
Transactions in System z

Transactions are regions of code starting with \textit{TBEGIN} and ending with \textit{TEND}.

- \textit{atomicity}  
  instructions within a transaction execute all or none

- \textit{isolation}  
  other CPUs or IO devices do not observe transaction’s memory updates, and transaction does not observe memory updates by other CPUs or IO  
  - isolation is \textit{strong}: transaction is isolated against other CPU’s non-transactional operations  
  - \textit{strong} isolation is imperative for realistic introduction of TX into existing software  
    abort & rollback if isolation cannot be guaranteed

- \textit{opacity: isolated in non-committed state}  
  transactions that abort are \textit{isolated} up to the point of abort  
  - another key requirement for introduction into existing software  
  - alternative \textit{validate} instruction to limit “zombie transactions” is too complex

- \textit{flattened nesting}  
  the entire nest of transactions is rolled back on abort  
  maximum nesting depth is 16
Use Cases for Transactional Execution

Three main use cases considered during definition phase:

- **Transactional Lock Elision**
  - replace lock acquire/release with transaction to ensure isolation of critical code section

  ```
  TRANSACTION BEGIN
  IF LOCK!=0 THEN ABORT
  .. perform critical section ..
  TRANSACTION END
  ```

  ```
  @abort:
  IF (count < threshold)
  retry transaction
  ELSE
  OBTAIN LOCK
  .. perform critical section..
  RELEASE LOCK
  ```

Benefits:
- reduced cache miss latency for exclusive fetch of lock-word cache line
- better scalability in false contention cases

- General code optimization
- Lock-free data structures
Use Cases for Transactional Execution

Three main use cases considered during definition phase:

- Transactional Lock Elision

- **General code optimization**
  - enable more aggressive compiler speculation, exploiting atomicity & isolation
  - aggressively optimize dominant code path, moving rare code paths into the transaction abort path

```c
IF (cond && C!=0)  
    A=B/C  
    STORE A, mem  
ELSE  
    ..  
ENDIF
```

```c
TRANSACTION BEGIN  
    A=B/C  
    ;; aborts if C=0  
    STORE A,mem ;; speculatively store  
    IF(!cond)  
        TABORT  
    TRANSACTION END
```

- Lock-free data structures
Use Cases for Transactional Execution

Three main use cases considered during definition phase:

- Transactional Lock Elision
- General code optimization
- **Lock-free data structures**
  - potential for rapid exploitation through common data structure libraries
  - transactions are easier / more powerful than Compare & Swap based algorithms
  - priority work queues, hash tables, double-linked lists, …
Transaction Aborts

- Successful TBEGIN sets Condition Code to 0 and executes sequential stream
- Transaction-abort returns to instruction after TBEGIN, with CC /= 0
  - CC=2 → likely transient condition, recommend retry (with threshold)
  - CC=3 → likely persistent condition, recommend fallback path

<table>
<thead>
<tr>
<th>Abort Code</th>
<th>Abort Reason</th>
<th>Condition Code</th>
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<tbody>
<tr>
<td>2</td>
<td>External interruption</td>
<td>2</td>
</tr>
<tr>
<td>4</td>
<td>Program interruption (unfiltered)</td>
<td>2 or 3</td>
</tr>
<tr>
<td>5</td>
<td>Machine-check interruption</td>
<td>2</td>
</tr>
<tr>
<td>6</td>
<td>I/O interruption</td>
<td>2</td>
</tr>
<tr>
<td>7</td>
<td>Fetch overflow</td>
<td>2 or 3</td>
</tr>
<tr>
<td>8</td>
<td>Store overflow</td>
<td>2 or 3</td>
</tr>
<tr>
<td>9</td>
<td>Fetch conflict</td>
<td>2</td>
</tr>
<tr>
<td>10</td>
<td>Store conflict</td>
<td>2</td>
</tr>
<tr>
<td>11</td>
<td>Restricted instruction</td>
<td>3</td>
</tr>
<tr>
<td>12</td>
<td>Program-interruption condition</td>
<td>3</td>
</tr>
<tr>
<td>13</td>
<td>Nesting depth exceeded</td>
<td>3</td>
</tr>
<tr>
<td>14</td>
<td>Cache fetch-related</td>
<td>2 or 3</td>
</tr>
<tr>
<td>15</td>
<td>Cache store-related</td>
<td>2 or 3</td>
</tr>
<tr>
<td>16</td>
<td>Cache other</td>
<td>2 or 3</td>
</tr>
<tr>
<td>255</td>
<td>Miscellaneous condition</td>
<td>2 or 3</td>
</tr>
<tr>
<td>&gt;256</td>
<td>TABORT instruction</td>
<td>2 or 3</td>
</tr>
</tbody>
</table>

\[
\text{LAI} R0,0  \quad \text{*initialize retry count=0}
\]

[loop]

TBEGIN  \quad \text{*begin transaction}

JNZ abort  \quad \text{*go to abort code if CC!=0}

LT R1,lock  \quad \text{*load test the fallback lock}

JNZ lockbusy  \quad \text{*branch if lock busy}

...perform operation...

TEND  \quad \text{*end transaction}

...

lockbusy TABORT  \quad \text{*abort if lock busy; this resumes after TBEGIN}

\[
\text{abort} J0 \quad \text{fallback} \quad \text{*no retry if CC=3}
\]

\[
\text{AH}\quad \text{R0,1} \quad \text{*increment retry count}
\]

CJNL R0,6,fallback  \quad \text{*give up after 6 attempts}

FFA R0,TX  \quad \text{*random delay based on retry count}

... potentially wait for lock to become free

\[
J \quad \text{loop} \quad \text{*jump back to retry}
\]

fallback

\[
\text{OBTAIN} \quad \text{lock} \quad \text{*using Compare&Swap}
\]

...perform operation...

RELEASE lock

...
Advanced TBEGIN features

Register save/restore
- TBEGIN General-Register-Save-Mask (GRSM) specifies which registers to save/restore
- Access and Floating Point Registers (AR/FPRs) are never saved/restored
  - A/F flag to avoid unintended overwriting of registers inside transaction

Program Interruption Handling
- Exceptions inside transaction abort and trap into OS
- Aggressive compiler optimization can lead to speculative program interruptions (unchecked pointers, unchecked data exceptions, etc)
- **Program Interruption Filtering Control (PIFC):**
  - Program can specify which classes of interrupts **not** to report to OS
  - Transaction still aborts, but without OS interrupt handler
Constrained Transactions

- Most transactions are expected to be short and touch few memory locations
  - in particular lock-free data structures, and many Java synchronized blocks (lock elision)
- Having to code & test fallback path is significant burden on software design & verification

- **Constrained Transactions**
  - always eventually complete
  - start with TBEGINC
  - no fallback path, CPU goes back to TBEGINC after abort

- List of constraints must be met, otherwise Constrained Exception detected
  - maximum data footprint of 4 x 32 Bytes
  - maximum of 32 assembler instructions, no backward branches (i.e. no loops)
  - maximum code footprint of 256 bytes, non-overlapping with data footprint on 4K pages
Software RAS & Debugging Features

- Software RAS & debugging are essential for enterprise class hardware & software
- Transactions pose serious problems
  - state (partially) rolled back at abort → new corner cases with aborts at different points
  - limited visibility of why abort occurred (e.g. access exception)
  - no ability to instruction-step through transaction

- TBEGIN can have *Transaction Diagnostic Block* parameter to store abort information
  - detailed abort code & hardware-internal abort reason
  - instruction & conflict address
  - General Register content before abort

- Enhancements for break- & watch-points
  - programmable to suppress events inside transactions, trigger at TEND

- Transaction Diagnostic Control
  - force random aborts to increase code verification coverage
Transaction Cache Management

- L1-Data Cache Unit tracks transactional footprint
  - new state bits for each 256 byte cache line
    - tx-read bit set during execution
    - tx-dirty bit set during L1 write back

- Gathering Store Cache buffers stores before L2
  - 64 entries x 128 byte capacity
  - CAM compare for gathering
  - circular queue for write back

- Abort handling
  - clear pending stores from STQ
  - clear all tx stores from Gathering Store Cache
  - clear dirty cache lines from L1

- L1/L2 track MESI-invalidations from L3 against TX footprint
  - reject: “stiff-arm” other CPU to try finish transaction
  - Abort transaction after reject thresholds
Implementation of Constrained Transactions

- Most constrained transactions complete on 1st or 2nd attempt without special handling
- Elaborate mechanisms implemented to guarantee eventual progress on repeated aborts
  - artificial instruction streams, e.g. self-modifying code around transaction
    - step-wise reduction of pipeline speculation in CPU
    - disable branch prediction, out-of-order execution, pipelining
  - unnaturally high contention or artificial instruction streams
    - disable speculative fetching
    - introduce random delays, tailored to specific machine circumstances
    - interlock conflicting processors in LPAR or system-wide
- Escalation modes controlled by millicode, adjust with number of aborts & system specifics
- Lab bring-up found very interesting harmonics, with as few as 2 and as many as 100 CPUs
- Similar machine-specific delays are available for non-constrained transactions
- *Perform Processor Assist (PPA-TX)* instruction
  - introduces random delay optimal for abort count and system specifics
  - prevents adjustments of software to CPU generation or system size
Performance Measurements

(a) TX vs locks, four variables, pool sizes 1k/10k
Performance Measurements

(d) TX vs read-write lock, four variables read, poolsize 10k
Summary

- System z is first commercially available general-purpose platform for Transactional Memory
- Architected with software reliability, debug ability, and future compatibility in mind
- Implementation without disrupting existing CPU and SMP micro-architecture
- Micro-benchmarks show scalability potential versus fine and coarse grained locks

- Software team finding more and more exploitation scenarios:
  - IBM XL C/C++ compiler support
    - published comparison of pthread locks vs transactions on subset of STAMP
  - z/OS Real Storage Manager lock avoidance
  - IBM Java ConcurrentLinkedQueue using Constrained Transactions
    - near-linear speed-up with number of CPUs
  - future IBM Java using lock elision
  - future IBM compilers to exploit general code reordering optimization using TX

- TX very promising tool to enable new wave of hardware & software co-innovation
Thank You

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6 cores per chip CP chip
6 CP chips + 2SC chips per MCM
Up to 4 MCMs

Four level cache hierarchy
- private L1/L2 store through 96KB+1MB data, 64KB+1MB itext
- shared L3/L4 caches store-in 48MB+384MB
- Inclusive caches: \( L_1 \subseteq L_2 \subseteq L_3 \subseteq L_4 \)

variant of MESI protocol
- “Cross Interrogate” (XI) between caches to invalidate cache lines
  - reject XI if hit against pending store
  - LRU-XI when higher-level cache evicts cache line
Pipeline

1. **Instr (clump)**
   - **D1**
   - **D2**

2. **IDU**
   - **IQ**
     - **G1**
       - **VQ wrt**
       - **Queue**
       - **Group**
     - **G2**
       - **Crack**
     - **M0**
       - **Cam**
     - **M1**
       - **Map**
     - **M2**
       - **Dep mtrx wrt**

3. **ISU**
   - **M3**
     - **S0**
     - **S1**
     - **S2**

4. **Regfile read**
   - **VBU (2)**
     - **A1**
     - **A0**
     - **A1**
     - **A2**
   - **LSU (2)**
     - **A0**
     - **A1**
     - **A2**
     - **A3**
     - **A4**
     - **A5**
   - **FXU (2)**
     - **A1**
     - **A0**
     - **A1**
     - **A2**
     - **A3**
     - **A4**
     - **A5**

5. **Out of order execution**

6. **Completion**
   - **N-1**
   - **N0**
   - **N1**
   - **N2**
   - **N3**
   - **R0**
   - **R1**
   - **R2**
   - **R3**
   - **R4**

7. **BFU**
   - **F0**
   - **F1**
   - **F2**
   - **F3**
   - **F4**
   - **F5**
   - **F6**
   - **F7**
   - **F8**
   - **WB**

8. **DFU**
   - **F1**
   - **F2**
   - **WB**
   - **Fin**
Key components of TX implementation

- **Instruction Decode Unit**
  - detects & cracks TBEGIN/TEND
  - counts nesting depth, tracks A/F/PFIC
  - passes current tx-state into Issue Queue per µ-ops
  - detects restricted instructions and requests abort

- **Fixed Point Unit**
  - copies GPRs for restore on abort
  - read by millicode during abort-process to restore GPRs

- **Global Completion Table**
  - tracks transactional state per “group” of µ-ops
  - refreshes IDU on flush
  - updates “architected” TX state at TBEGIN/TEND completion
Other instructions

- **ETND**  Extract Transaction Nesting Depth
- **NTSTG**  Non-transactional store
  Gathering Store Cache has byte-mask of which bytes are transactional vs non-transactional. During abort, NTSTG’s stores survive.
- **PPA**  Perform random delay based on system characteristics.
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