The performance vulnerability of architectural and non-architectural arrays to permanent faults

Damien Hardy, Isidoros Sideris, Nikolas Ladas, Yiannakis Sazeides

University of Cyprus - University of Rennes 1/IRISA

MICRO 45, Vancouver, December 3rd, 2012
Permanent faults & failure

- Tomorrow
  - Failure will not be exceptional
    - Pfail increases with scaling

- Making hardware perfect not scalable
  - Increase spares  => more area/cost
  - Larger cells    => more area/power/cost

- Solution: Finer Disabling Grain
  => A processor that operates correctly in the presence of permanent faults by disabling faulty entries

The performance vulnerability of architectural and non-architectural arrays to permanent faults
Measure Performance Variability (PV)

- Implication of Permanent Faults on Performance
  - What is the expected performance of such processor?
  - What is the performance distribution of such a processor?
  - Which arrays are more critical to protect?

- Current practice: Measure PV for a given $p_{fail}$ with fault maps
  - How many fault maps to generate to get accurate results?
  - A lot of computation time may be required

The performance vulnerability of architectural and non-architectural arrays to permanent faults
Analytical based methodology

- Rapid estimation of expected PV and PV distribution
  - Without many and long microarchitectural simulations
  - Without fault map generation

- Enables designer to
  - Determine which structures are more important to protect
  - Explore reliability based trade-offs

**Session IB - Fault Tolerance**

The performance vulnerability of architectural and non-architectural arrays to permanent faults