CALL FOR PARTICIPATION
MICRO - 41
November 8 - 12, 2008  Lake Como, Italy
The 41st Annual IEEE/ACM International Symposium on Microarchitecture

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Co-sponsored by IEEE-CS TC-uARCH and ACM SIGMICRO

Important Dates: Paper acceptance: August 5, Early registration closes: October 6

The 41st International Symposium on Microarchitecture is the premier forum for presenting, discussing, and debating innovative microarchitecture ideas and techniques for advanced computing and communication systems. This symposium brings together researchers in fields related to microarchitecture, compilers, chips, and systems for technical exchange on traditional microarchitecture topics and emerging research areas. The MICRO community has enjoyed a close interaction between academic researchers and industrial designers and we aim to continue this tradition at MICRO-41.

Conference program summary:
- Nov 8 – 9: Workshops and Tutorial sessions
- Nov 10 – 12: Technical paper presentations (technical program will be available on September 1, 2008)
- Keynotes by David E. Shaw, Chief Scientist, D.E. Shaw Research and Charles R. Moore, Senior Fellow, AMD
- Activities: Lake boat tour and gala dinner at the Società del Casino in Como

The conference is hosted in the Spazio Como conference center of the Grand Hotel di Como (http://www.grandhoteldicomo.com/).

For more information please consult the conference website:
http://www.microarch.org/micro41
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Workshops (Nov 8 – 9):
- dasCMP: Workshop on Design, Architecture and Simulation of Chip Multi-Processors
  Norman Jouppi, Rakesh Kumar, and Dean Tullsen
- **Streaming Systems**: From Web and Enterprise to Multicore
  Rodric Rabbah, Xiaowei Shen, and Saman Amarasinghe
- **New Frontiers in High-performance and Hardware-aware Computing (HipHac)**
  Rainer Buchty and Jan-Philipp Weiß
- **3rd Workshop on Dependable Architecture (WDA-3)**
  Osman S. Unsal, Oguz Ergin, and Yiannakis Sazeides
- **Network on Chip Architectures (NoCArc)**
  Maurizio Palesi and Shashi Kumar

Tutorials (Nov 8 – 9):
- **Programming Throughput-Oriented Architectures with Ct**
  Anwar Ghuloum, Gansha Wu and Xin Zhou
- **On-Chip Communication Architectures: Busses, Networks-on-Chip and Beyond**
  Nikil Dutt, Luca Benini, and Sudeep Pasricha
- **Coherence and Memory Consistency Models**
  Michel Dubois
- **VLIW Compilation Environment and Multi-Processor Architecture of Diopss, the RISC+ floating-Point VLIW DSP System-On-Chip Designed for High Quality Acoustic Applications**
  Gert Goossens, Pier Stanislao Paolucci and Piergiovanni Bazzana
- **COTSOn: Infrastructure for System-Level Simulation**
  Theresa Frawley, Vincent Lim, Ayose Falcon, Paolo Faraboschi and Daniel Ortega
- **Design Variability: Trends, Models, and Design Solutions**
  Keith Bowman, David Brooks, Gu-Yeon Wei and Chris Wilkerson
- **Performance Tools for Understanding the Behavior of Running Programs on the Cell B.E**
  Bilha Mendelson, Gadi Haber and Thomas Chen
- **Modeling, Verification and Mapping of Applications on WSN Architectures**
  Franco Fummi, Andrea Acquaviva, Davide Quaglia and Giovanni Perbellini
- **Microprocessor Memory Array Circuits for Architects**
  Shih-Lien Lu, Dinesh Somasekhar and Steven Hsu
- **Changing Factors in Memory System Design**
  Kenneth Wright and Hillery Hunter
- **CAD Solutions for System-Level Power Optimization**
  Enrico Macii and Massimo Poncinno

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