Tutorial/Workshop Program at a Glance

	Saturday 4th			Sunday 5th			
	Real-time 3D Graphics Architecture Tutorial	Virtual Machines: Architectures, Implementations and Applications Tutorial	Low Power Robust Computing Tutorial	Compilation System for throughput driven mulit-core processors Tutorial	Power Aware Computer Systems Workshop	Media and Stream Processors Workshop	Branch Prediction Contest
Venue	Morrison	Broadway	Sellwood / Ross Island	Three Sisters	Mount Bachelor	Mount Hood	Mount St. Helens
8:00 Breakfast (Holladay East)							
8:30 Morning Session 1	X	X	X	X	X	X	
10:00 Break (Holladay East)							
10:30 Morning Session 2	X	X	X	X	X	X	
12:00 Lunch (Oregon Room – part of Pacific NW Ballroom)				12:00 Lunch (Pacific NW Ballroom)			
13:00 Afternoon Session 1		X	X		X	X	X
14:30 Break (Holladay East)							
15:00 Afternoon Session 2		X	X		X	X	X
				18:00 Pre-conference Reception and Dinner. Venue: Pacific NW Ballroom			

Tutorials

Real-time 3D Graphics Architecture. William R. Mark (U. Texas, Austin), Henry Moreton (NVIDIA).
Room: Morrison, Saturday 12/4. 8:30 – 12:00.

Virtual Machines: Architectures, Implementations and Applications. Jim E. Smith (U. Wisconsin, Madison), Ravi Nair (IBM Research).
Room: Broadway, Saturday 12/4. 8:30 – 17:00.

Low Power Robust Computing. Todd Austin, David Blaauw, Trevor Mudge, Dennis Sylvester (U. Michigan), Krisztian Flautner (ARM Ltd.), Nam Sung Kim (Intel).
Room: Sellwood/Ross Island, Saturday 12/4. 8:30 – 17:00.

Compilation system for throughput-driven multi-core processors. Michael Chen, Erik Johnson, Roy Ju (Intel).
Room: Three Sisters, Sunday 12/5. 8:30 – 12:00.

Workshops

Workshop on Power-Aware Computer Systems (PACS'04). Babak Falsafi (CMU), T. N. Vijaykumar (Purdue U.).
Room: Mount Bachelor, Sunday 12/5. 8:30 – 16:30.

6th Workshop on Media and Stream Processors (MSP6).
Room: Mount Hood, Sunday 12/5. 8:30 – 17:00.

Branch Prediction Contest/Championship Branch Prediction (CBP-1).
Room: Mount St. Helens, Sunday 12/5. 13:30 – 17:00.