Microarchitecture and Design Challenges for Gigascale Integration

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Abstract

VLSI system performance increased by five orders of magnitude in the last three decades, made possible by continued technology scaling, improving transistor performance to increase frequency, increasing integration capacity to realize complex architectures, and reducing energy consumed per logic operation to keep power dissipation within limit. The technology treadmill will continue, providing integration capacity of billions of transistors; however, power, energy consumption, and variations will be the barriers. Performance at any cost will not be an option in the future; VLSI systems will have to emphasize performance delivered in a given power envelope, with complexity limited by energy efficiency and variability. This talk will discuss potential solutions in process technology, circuits, and microarchitectures to exploit future gigascale integration capacity. The system on a chip (SOC) concept will help integrate diverse functional blocks, providing valued performance. The talk will conclude with recommendations to the VLSI system designers and microarchitects on how to exploit these emerging paradigms.

Shekhar Borkar graduated with an MS in Physics from University of Bombay, MSEE from University of Notre Dame in 1981, and joined Intel Corporation. He worked on the 8051 family of microcontrollers, the iWarp multicomputer project, and subsequently on Intel's supercomputers. He is an Intel Fellow and director of Circuit Research. His research interests are high performance and low power digital circuits, and high-speed signaling. Shekhar is an adjunct faculty member at Oregon Graduate Institute, and teaches VLSI design.